

LED Driver IC

EXC2668L

DESCRIPTION

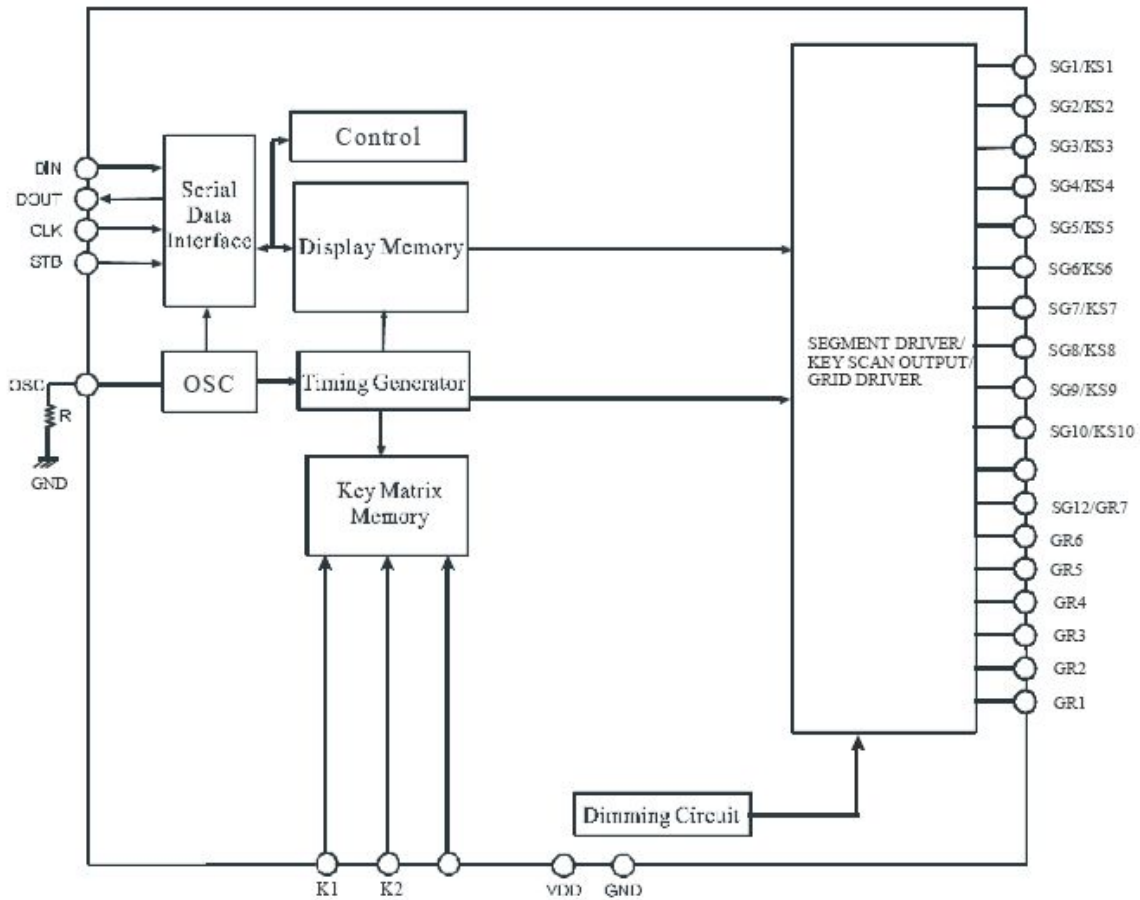
EXC2668 is an LED Controller driven on a 1/7 to 1/8 duty factor. Ten segment output lines, six grid output lines, 1 segment/grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to EXC2668 via a four-line serial interface. Housed in a 28-pin SO Package, EXC2668 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

FEATURES

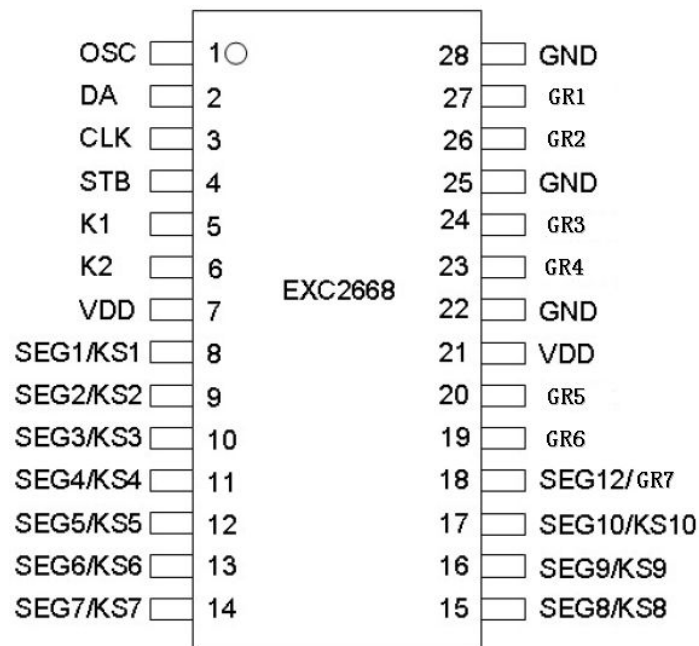
- CMOS Technology
- Low Power Consumption 5V
- Multiple Display Modes (10segment, 7Grid to 11segment, 6Grid)
- Key Scanning (10 x 2 Matrix)
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- RC oscillator inside
- POR Circuit inside
- Available in 28-pin, SOP Package

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BLOCK DIAGRAM:



PIN CONFIGURATION:



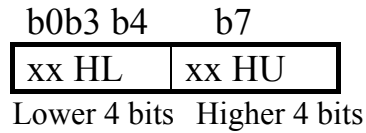
PIN DESCRIPTION:

PinName	I/O	PinNo.	Description
OSC	I	1	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency(100K~150K)
DIN	I	2	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)
DOUT	O	2	DataOutputPin (N-Channel , Open-Drain)This pin outputs serial data at the falling edge of the shift clock.
STB	I	4	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command . When this pin is "HIGH ",CLK is ignored .
CLK	I	3	C lock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.
K1~K2	I	6~7	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)
Seg1/KS1~ Seg10/KS10	O	8~17	Segment Output Pins (p-channel , open drain) Also acts as the Key Source
Grid1~ Grid6	O	27,26,24 23,20,19	Grid Output Pins
Seg12/Grid7	O	18	Segment/Grid OutputPins
VDD	-	7,21	Power Supply 5V ± 10%
GND	-	28,25,22	Ground Pin

DISPLAY MODE AND RAM ADDRESS:

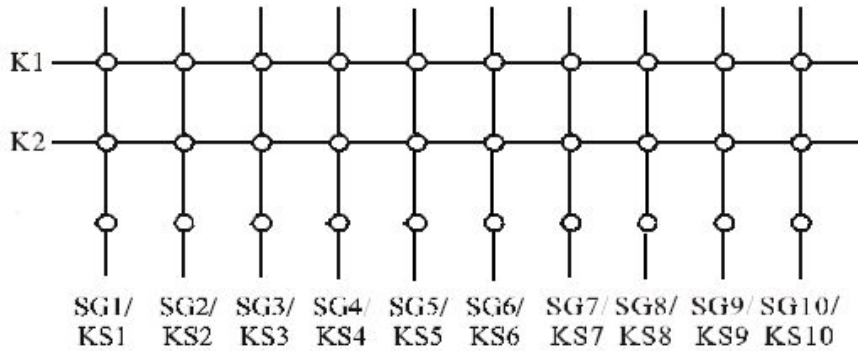
Data transmitted from an external device to EXC2668 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM addresses of EXC2668 are given below in 8 bits unit.:

Seg1	Seg8	Seg9	Seg12	
00HL	00HU	01HL	01HU	DIG1
02HL	02HU	03HL	03HU	DIG2
04HL	04HU	05HL	05HU	DIG3
06HL	06HU	07HL	07HU	DIG4
08HL	08HU	09HL	09HU	DIG5
0AHL	0AHU	0BHL	0BHU	DIG6
0CHL	0CHU	0DHL	0DHU	DIG7

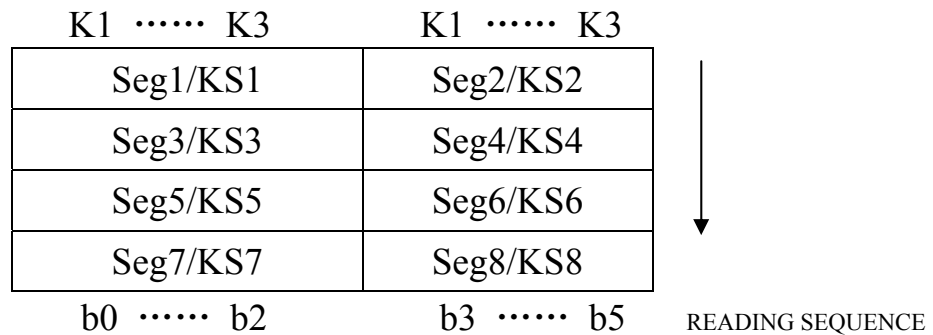


KEY MATRIX & KEY INPUT DATA STORAGE RAM(K3 pin is null):

EXC2668 Key Matrix consists of 10 x 2 array as shown below:



Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b0) has been read, the least significant bit of the next data (b7) is read.:



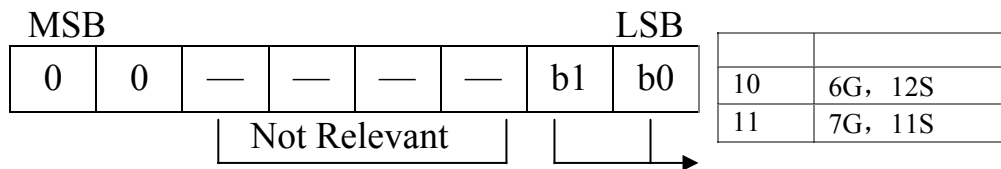
FUNCTIONAL DESCRIPTION:

A command is the first byte (b0 to b7) inputted to EXC2668 via the DIN Pin after STB Pin has changed from HIGH to LOW State. If for some reason the STB Pin is set to HIGH while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

(1) Display Mode Setting Commands:

EXC2668 provides 2 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to EXC2668 via the DIN Pin when STB is LOW. However, for these commands, the bit 3 to bit 6 (b2 to b5) are ignored, bit 7 & bit 8 (b6 to b7) are given a value of 0.

The Display Mode Setting Commands determine the number of segments and grids to be used(12 to 14segments, 4 to 6 grids). A display command ON must be executed in order to resume display. If the same mode setting is selected, no command execution is take place,therefore, nothing happens.

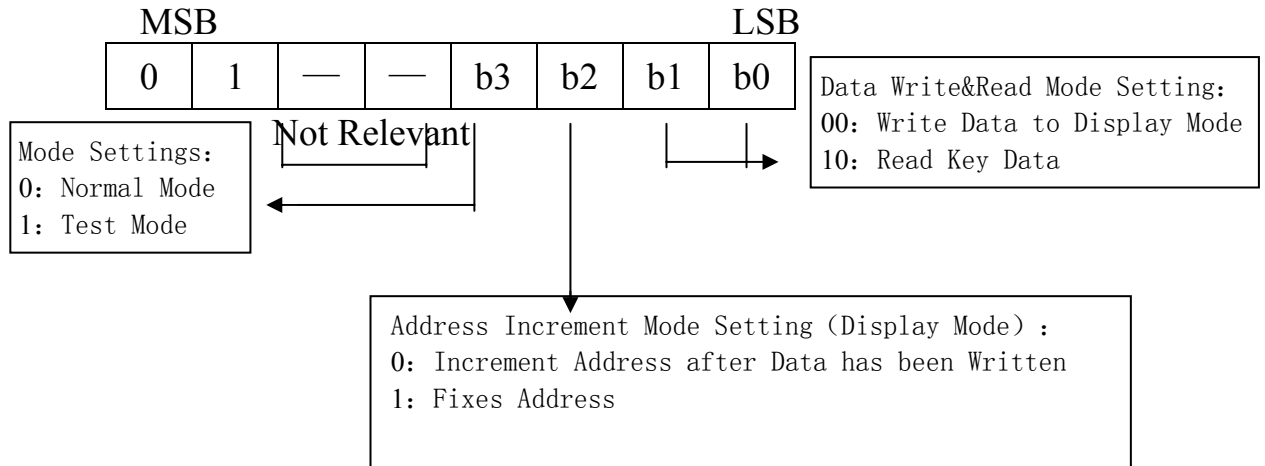


When Power is turned ON, the 7-grid , 11-segment modes is selected.

(2) Data Setting Commands:

The Data Setting Commands executes the Data Write or Data Read Modes for EXC2668. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of 1 while bit 8 (b7) is given the value of 0. Please refer to the diagram below.

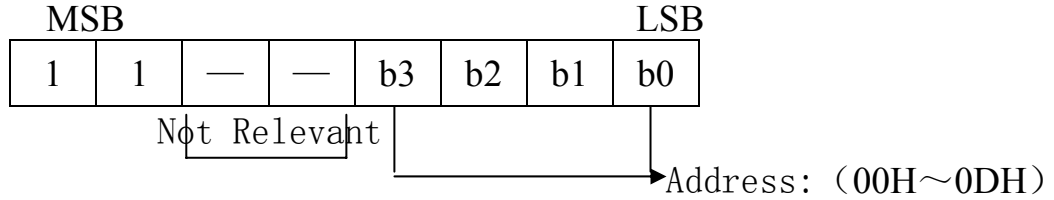
When poweris turned ON, bit 4 to bit 1 (b3 to b0) are given the value of 0.



(3) Address Setting Commands:

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH.

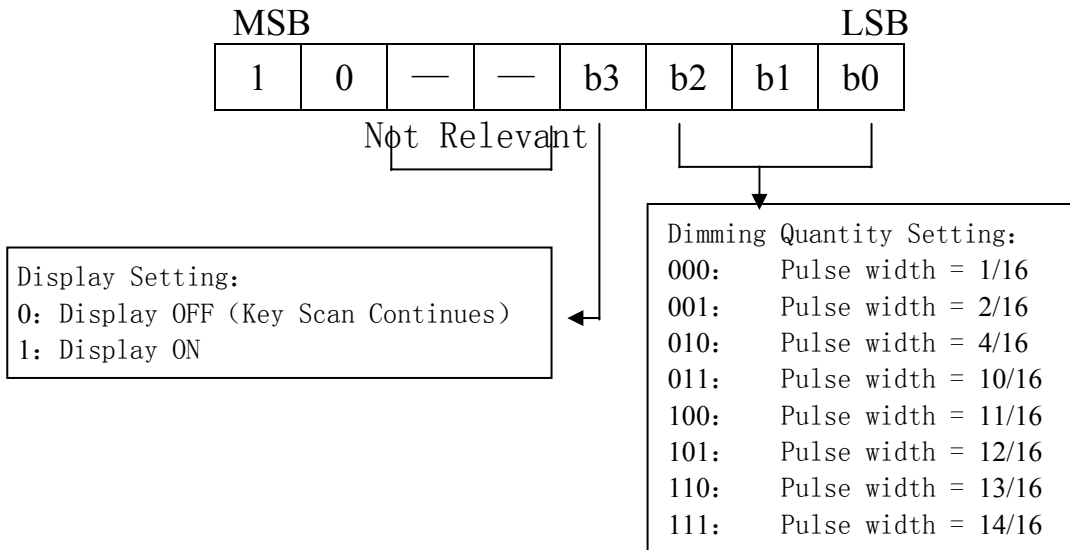
Please refer to the diagram below.



If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at 00H.

(4) Display Control Commands:

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below.

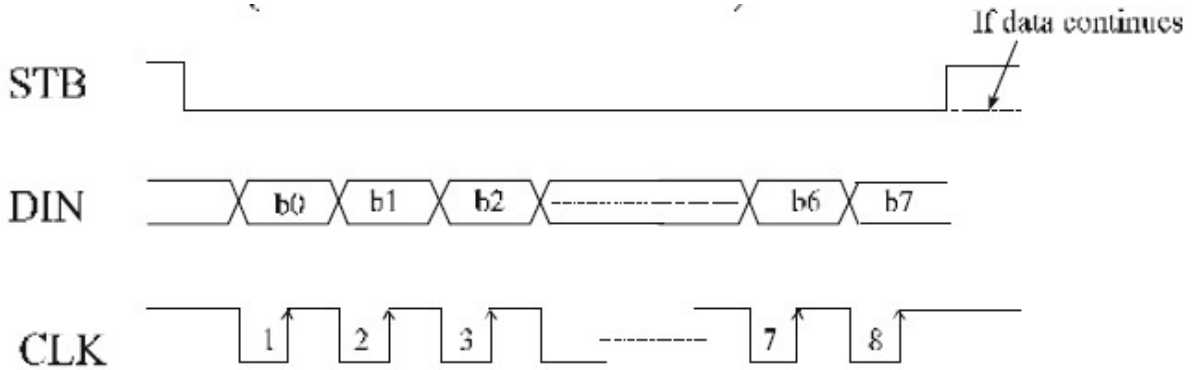


When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is started).

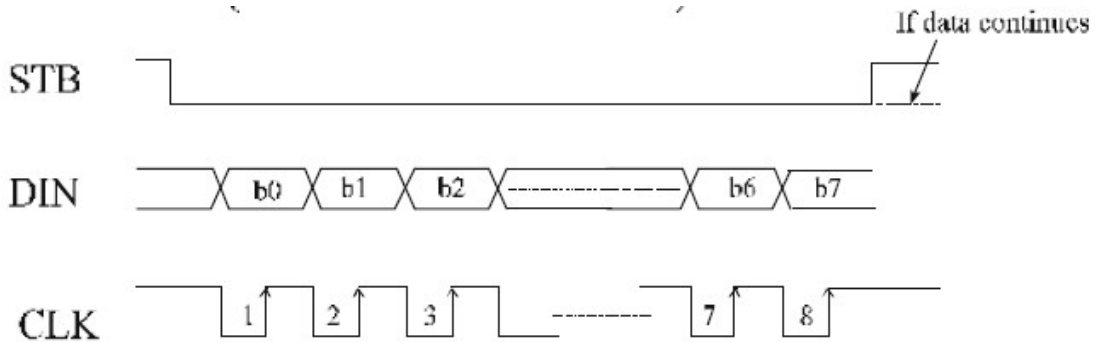
SERIAL COMMUNICATION FORMAT:

The following diagram shows the EXC2668 serial communication format. The DOUT Pin is an N-channel, opendrain output pin, therefore, it is highly recommended that an external pull-up resistor (4.7 KOhms to 10 KOhms) must be connected to DOUT.

Data/Command Write



Data Read:

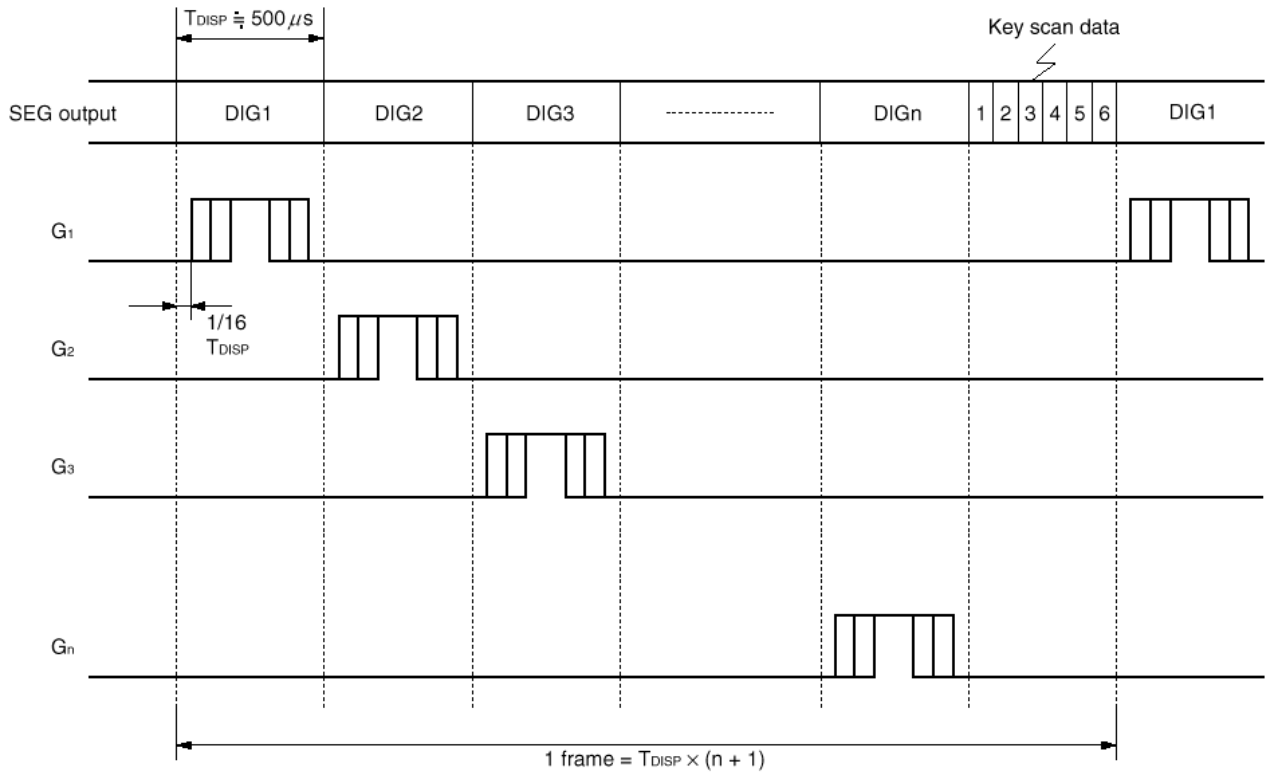


where: t_{wait} (waiting time) $\geq 1\mu s$

It must be noted that when the data is read, the waiting time (t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to $1\mu s$.

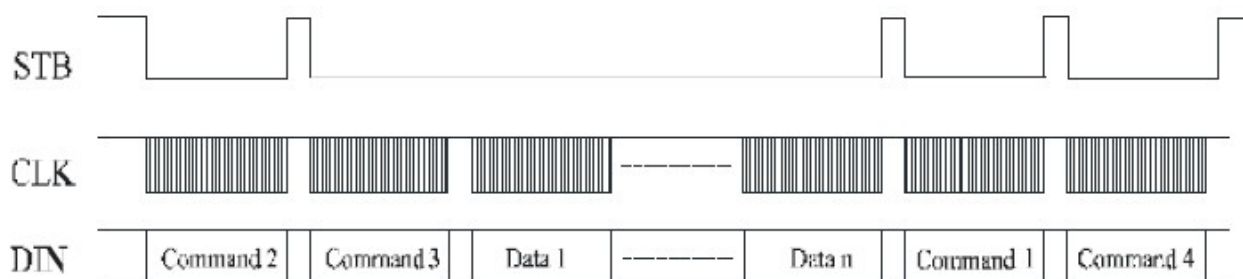
SCANNING AND DISPLAY TIMING:

The Key Scanning and Display Timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the are 10 x 3 matrix is stored in the RAM.



APPLICATIONS:

(1) addresses incrementing model.



Command1: Display Mode Setting Command
 Command2: Data Setting Command
 Command3: Address Setting Command
 Data1 ~ n: Transfer Display Data (14 Bytes max.)
 Command4: Display Control Command

(2) specific addresses model



Command1: Data Setting Command
 Command2: Address Setting Command
 Data : Display Data

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$, $Gnd = 0\text{ V}$)

Parameter	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.5 ~ +7.0	V
Logic Input Voltage	VI1	-0.5 ~ VDD + 0.5	V
LED Seg Output Driver Current	IO1	-50	mA
LED Grid Output Driver Current	IO2	+200	mA
Power	PD	400	mW
Operating Temperature	Topt	-40 ~ +80	°C
Storage Temperature	Tstg	-65 ~ +150	°C

RECOMMENDED OPERATING RANGE($T_a = -20 \sim +70^\circ\text{C}$, $Gnd = 0\text{ V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	VDD		5		V
High-Level Input Voltage	VIH	0.7 VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.3 VDD	V

ELECTRICAL CHARACTERISTICS($T_a = -20 \sim +70^\circ\text{C}$, $VDD = 4.5 \sim 5.5\text{ V}$, $Gnd = 0\text{ V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
High-Level Output Current	Ioh1	-20	-25	-40	mA	Seg1 – Seg10, $v_o = v_{dd}-2V$
	Ioh2	-20	-30	-50	mA	Seg1 – Seg10, $v_o = v_{dd}-3V$
Low-Level Output Current	IOL1	80	140	-	mA	Grid1 – Grid6 . $V_o=0.3V$
Low-Level Output Current	Idout	4	-	-	mA	$V_O = 0.4V$, dout

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Segment High-Level Output Current Tolerance	Itolsg	-	-	5	%	VO = VDD - 3V, Seg1~Seg11
PullDown Resistor	RL		10		KΩ	K1 - K3
Input Current	II	-	-	±1	μA	VI = VDD / VSS
High-Level Input Voltage	VIH	0.7 VDD	-		V	CLK, DIN, STB
Low-Level Input Voltage	VIL	-	-	0.3 VDD	V	CLK, DIN, STB
Delay Voltage	VH	-	0.35	-	V	CLK, DIN, STB
Dynamic Current	IDDdyn	-	-	5	mA	No Load, Display off

SWITCHING CHARACTERISTIC

(Ta = -20 ~ +70°C, VDD = 4.5 ~ 5.5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	
Oscillation Frequency	fosc	-	500	-	KHz		
Timing Delay	tPLZ	-	-	300	ns	CLK → DOUT	
	tPZL	-	-	100	ns	CL = 15pF, RL = 10 KΩ	
Rise time	TTZH1	-	-	2	μs	CL = 300pF	Seg1~Seg10
	TTZH2	-	-	0.5	μs		Grid1~Grid4 Seg12/Grid7~ Seg14/Grid5
Fall time	TTHZ	-	-	120	μs	CL = 300pF, Segn, Gridn	
Max frequency	Fmax	1	-	-	MHz	duty cycle 50%	
Input Cap	CI	-	-	15	pF	-	

*** TIMING CHARACTERISTICS**

($T_a = -20 \sim +70^\circ\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{ V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	TestCondition
Clock width	PWCLK	400	-	-	ns	-
STB width	PWSTB	1	-	-	μs	-
Setup Timing	tSETUP	100	-	-	ns	-
Hold TIMING	tHOLD	100	-	-	ns	-
CLK → STB Timing	tCLK STB	1	-	-	μs	CLK ↑ → STB ↑
Wait Timing	tWAIT	1	-	-	μs	CLK ↑ → CLK ↓

SWITCHING CHARACTERISTIC WAVEFORM:

