N-Channel Logic Level Enhancement Mode Power MOSFET

K3475N

BV_{DSS}		70	V
I_D@V_{GS}=10V,T_C=25°C		70	A
R_{DSON}(MAX)	V_{GS}=10V,I_D=40A	8.4	mΩ

100% ΔVds TESTED!

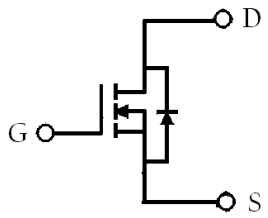
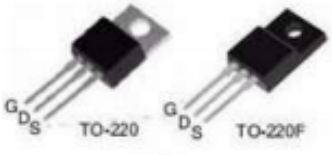
100% UIS TESTED!

Features

- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Description

The K3475N is the high cell density trenched N-ch MOSFETs, which provide excellent R_{DSON} and gate charge for most of the synchronous buck converter applications. The K3475N meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Equivalent Circuit	Outline
	**TO-220/TO-220F** 

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
K3475N	K3475N	TO-220/TO-220F			1000

Table 1. Thermal Characteristic

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	1.77	℃/W

Table 2. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (VGS=0V)	70	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±25	V
$I_{D\ (DC)}$	Drain Current-Continuous(Tc =25℃)	70	A
	Drain Current-Continuous(Tc =100℃)	47.6	
$I_{DM\ (pluse)}$	Drain Current-Continuous@ Current-Pulsed	272	A
P_D	Maximum Power Dissipation(Tc=25℃)	85	W
E_{AS}	Single Pulse Avalanche Energy	360	mJ
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	70			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=68V,V_{GS}=0V			1	μA
	Zero Gate Voltage Drain Current(Tc=100℃)	V_{DS}=68V,V_{GS}=0V			10	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±25V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2		4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=40A		7	8.4	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V f=1.0MHz		2708		PF
C_{oss}	Output Capacitance			353		PF
C_{rss}	Reverse Transfer Capacitance			168		PF
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	VDD=30V,ID=2A, RL=15Ω,VGS=10V, RG=2.5Ω		9		nS
t_r	Turn-on Rise Time			11		nS
$t_{d(off)}$	Turn-Off Delay Time			19		nS
t_f	Turn-Off Fall Time			23		nS

Q_g	Total Gate Charge	V_{DS}=50V, V_{GS}=10V, I_D=40A		64		nC
Q_{gs}	Gate-Source Charge			13.4		nC
Q_{gd}	Gate-Drain Charge			26.2		nC
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)			68		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			272		A
V_{SD}	Forward On Voltage	I_{SD}=40A,V_{GS}=0V		0.79	0.95	V
t_{rr}	Reverse Recovery Time	T_J=25℃I_F=75A, di/dt=100A/μs		34		nS
Q_{rr}	Reverse Recovery Charge			69		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated				

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width≦300us , duty cycle≦2%

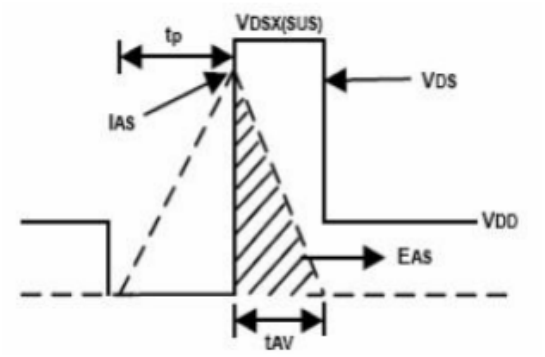
3.The EAS data shows Max. rating . The test condition is V_{DD} =25V,V_{GS} =10V,L=0.1mH

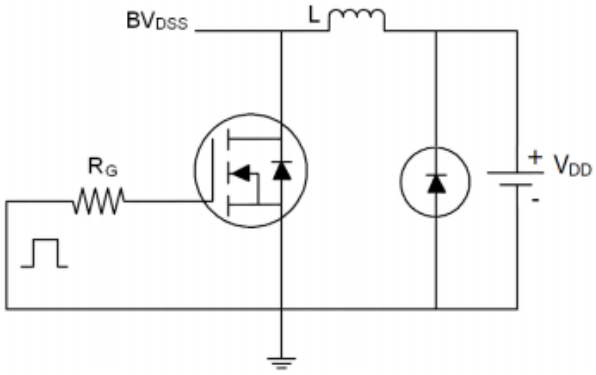
4.The power dissipation is limited by 175℃ junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

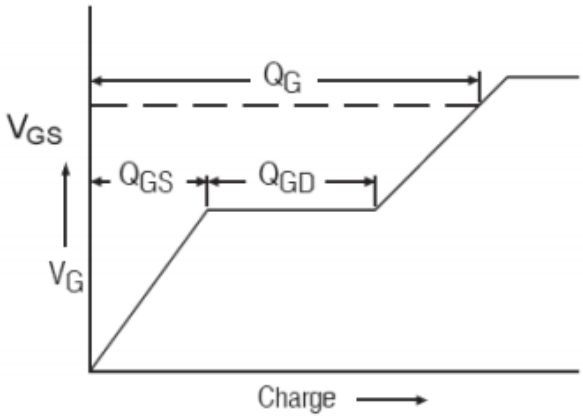
TEST CIRCUIT

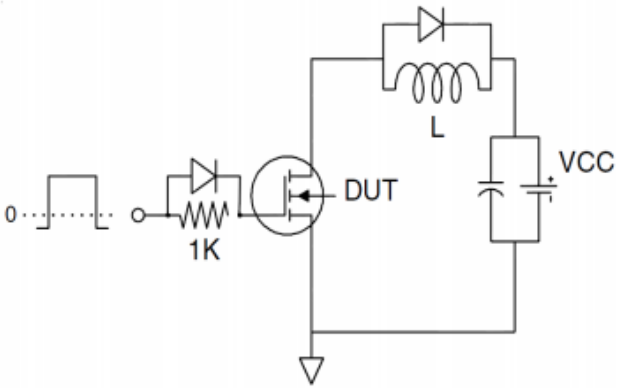
1）E_{AS} Test Circuits



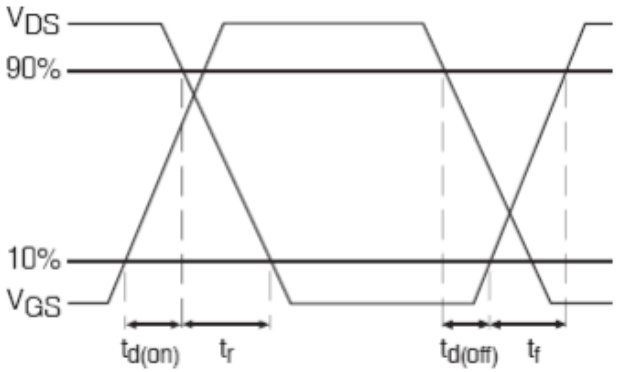


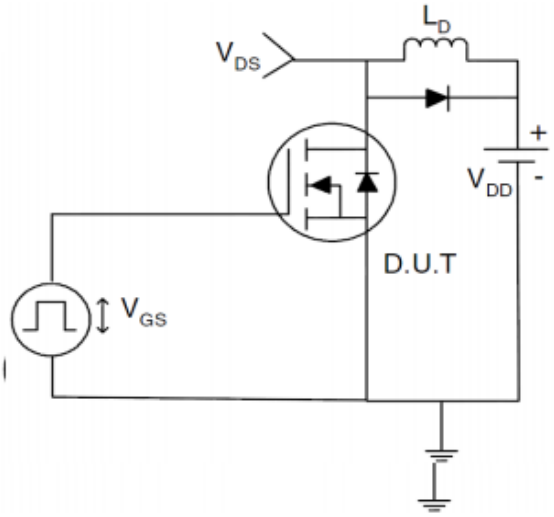
2）Gate Charge Test Circuit:





3）Switch Time Test Circuit:





TYPICAL CHARACTERISTICS

Figure1. Safe Operating Area

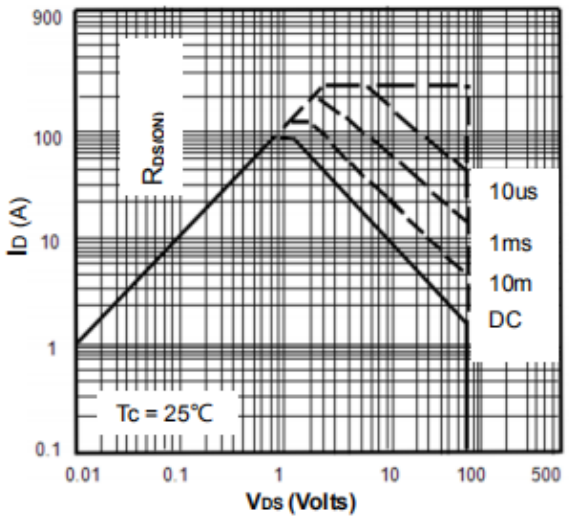


Figure2. Source-Drain Diode Forward Voltage

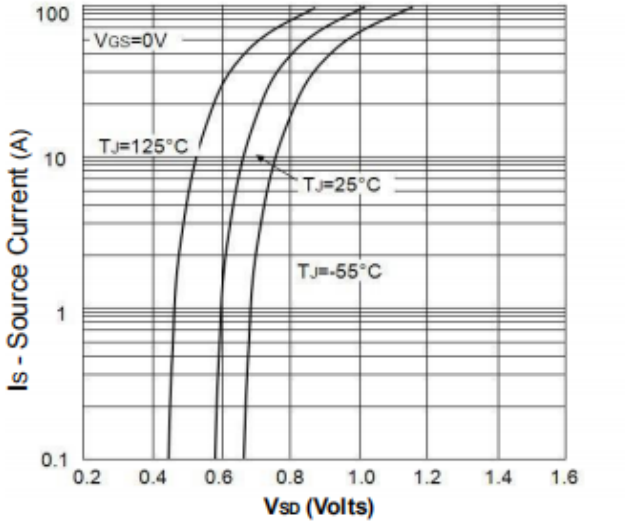


Figure3. Output Characteristics

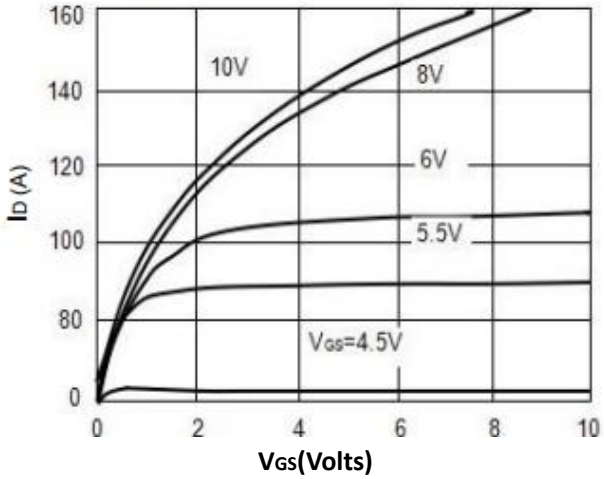


Figure4. Transfer Characteristics

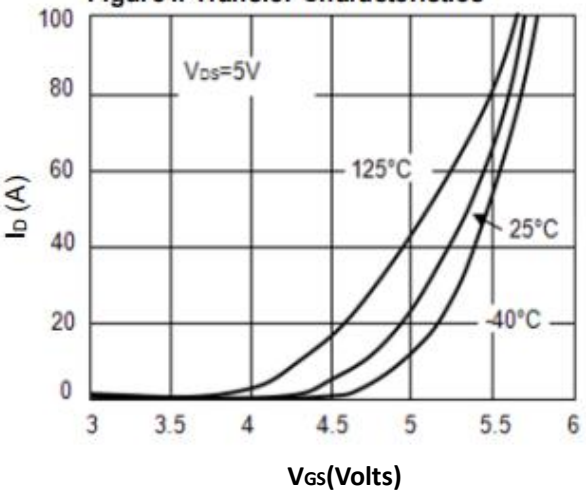


Figure5. Static Drain-Source On Resistance

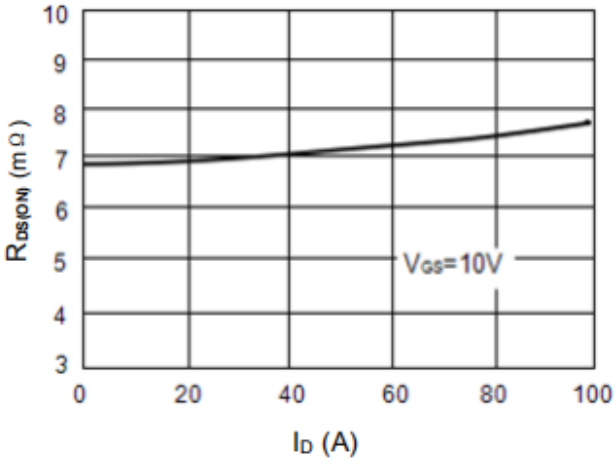


Figure6. $R_{DS(ON)}$ vs Junction Temperature

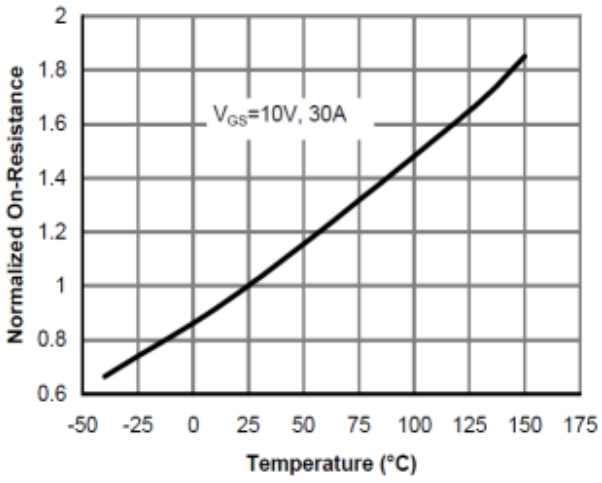


Figure7. BV_{DSS} vs Junction Temperature

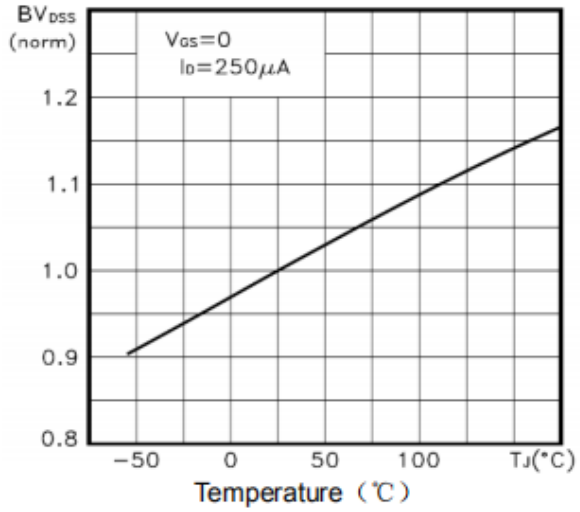


Figure8. $V_{GS(th)}$ vs Junction Temperature

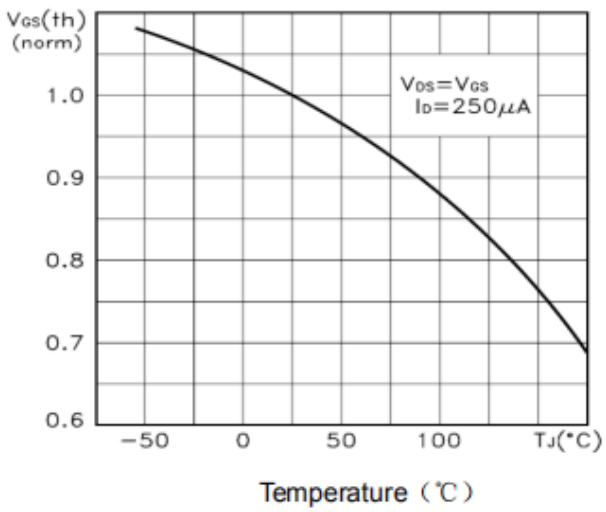


Figure9. Gate Charge Waveforms

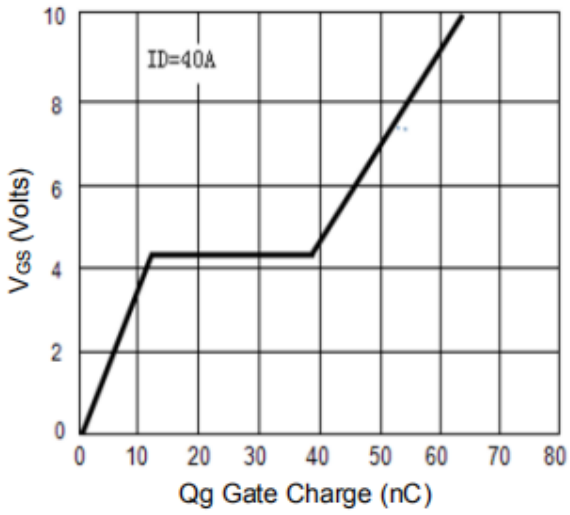


Figure10. Capacitance

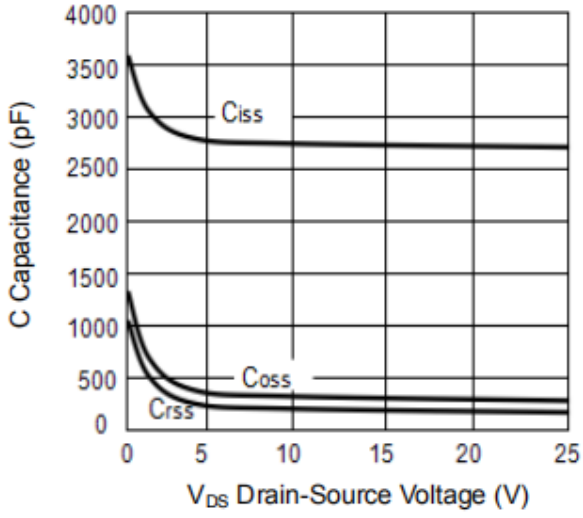
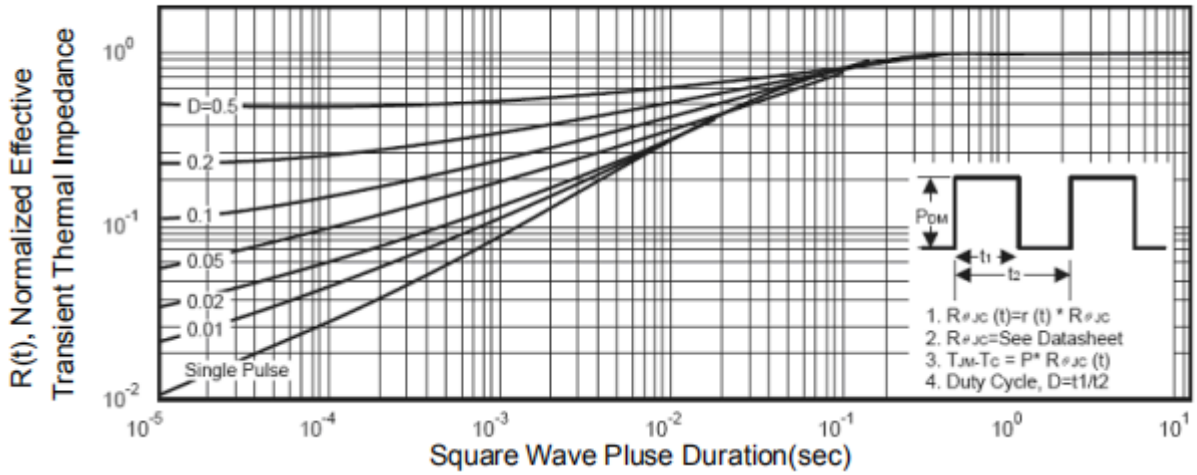
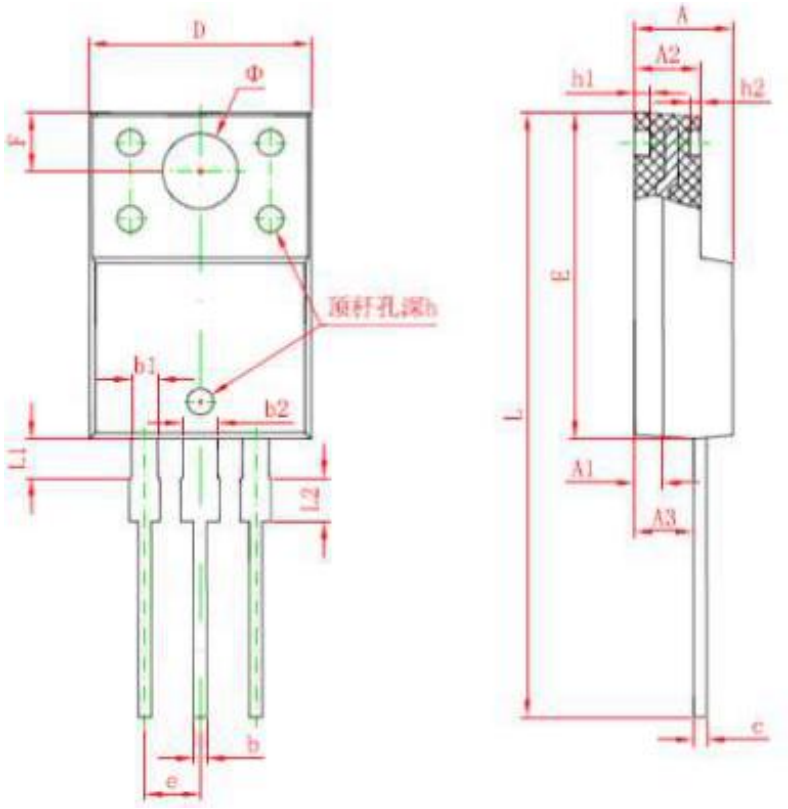


Figure11. Normalized Maximum Transient Thermal Impedance

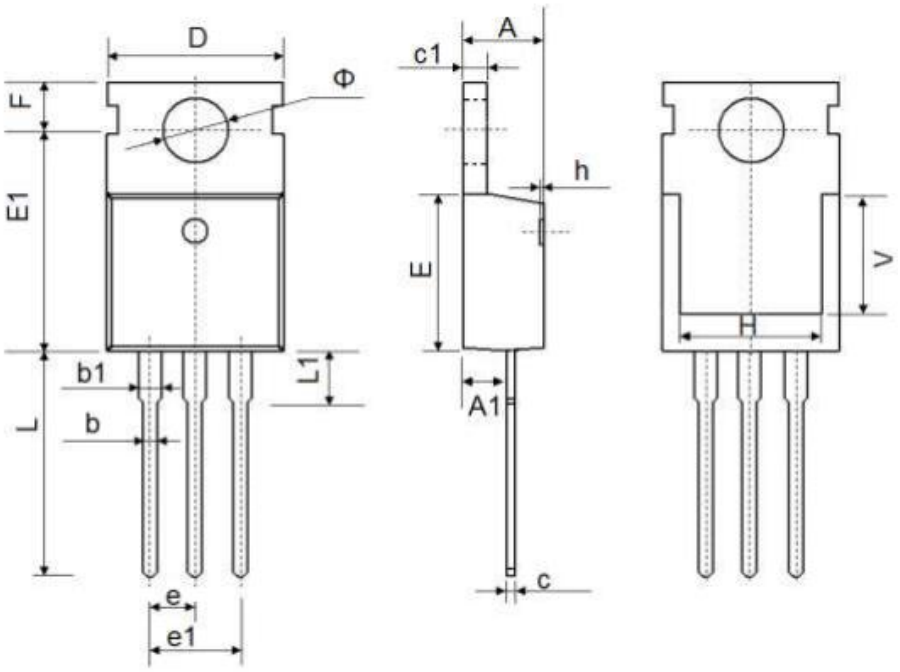


TO-220F PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.300	4.700	0.169	0.185
A1	1.300 REF.		0.051 REF.	
A2	2.800	3.200	0.110	0.126
A3	2.500	2.900	0.098	0.114
b	0.500	0.750	0.020	0.030
b1	1.100	1.350	0.043	0.053
b2	1.500	1.750	0.059	0.069
c	0.500	0.750	0.020	0.030
D	9.960	10.360	0.392	0.408
E	14.800	15.200	0.583	0.598
e	2.540 TYP.		0.100 TYP.	
F	2.700 REF.		0.106 REF.	
Φ	3.500 REF.		0.138 REF.	
h	0.000	0.300	0.000	0.012
h1	0.800 REF.		0.031 REF.	
h2	0.500 REF.		0.020 REF.	
L	28.000	28.400	1.102	1.118
L1	1.700	1.900	0.067	0.075
L2	1.900	2.100	0.075	0.083

TO-220 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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