

# LMV331, NCV331, LMV393, LMV339

## Single, Dual, Quad General Purpose, Low Voltage Comparators

The LMV331 is a CMOS single channel, general purpose, low voltage comparator. The LMV393 and LMV339 are dual and quad channel versions, respectively. The LMV331/393/339 are specified for 2.7 V to 5 V performance, have excellent input common-mode range, low quiescent current, and are available in several space saving packages.

The LMV331 is available in 5-pin SC-70 and TSOP-5 packages. The LMV393 is available in a 8-pin Micro8™, SOIC-8, and a UDFN8 package, and the LMV339 is available in a SOIC-14 and a TSSOP-14 package.

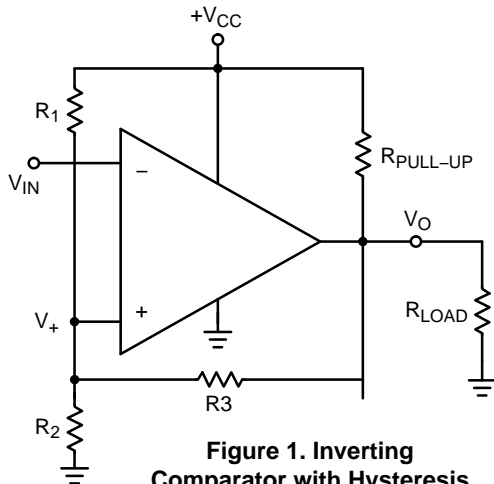
The LMV331/393/339 are cost effective solutions for applications where space saving, low voltage operation, and low power are the primary specifications in circuit design for portable applications.

### Features

- Guaranteed 2.7 V and 5 V Performance
- Input Common-mode Voltage Range Extends to Ground
- Open Drain Output for Wired-OR Applications
- Low Quiescent Current: 60  $\mu$ A/channel TYP @ 5 V
- Low Saturation Voltage 200 mV TYP @ 5 V
- Propagation Delay 200 ns TYP @ 5 V
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Battery Monitors
- Notebooks and PDA's
- General Purpose Portable Devices
- General Purpose Low Voltage Applications



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**SC-70  
CASE 419A**



**TSOP-5  
CASE 483**



**Micro8  
CASE 846A**



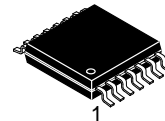
**SOIC-8  
CASE 751**



**UDFN8  
CASE 517AJ**



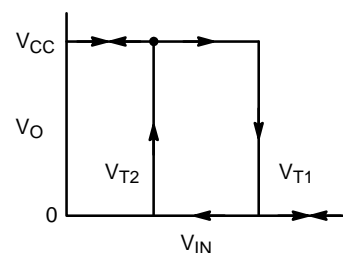
**SOIC-14  
CASE 751A**



**TSSOP-14  
CASE 948G**

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

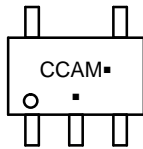


**Figure 2. Hysteresis Curve**

# LMV331, NCV331, LMV393, LMV339

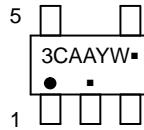
## MARKING DIAGRAMS

**SC-70  
CASE 419A**



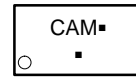
CCA = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

**TSOP-5  
CASE 483**



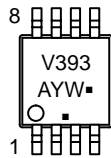
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

**UDFN8  
CASE 517AJ**



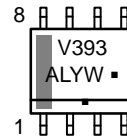
CA = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

**Micro8  
CASE 846A**



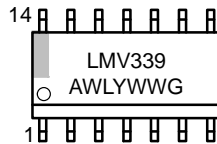
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

**SOIC-8  
CASE 751**



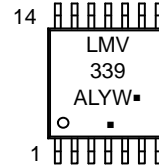
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

**SOIC-14  
CASE 751A**



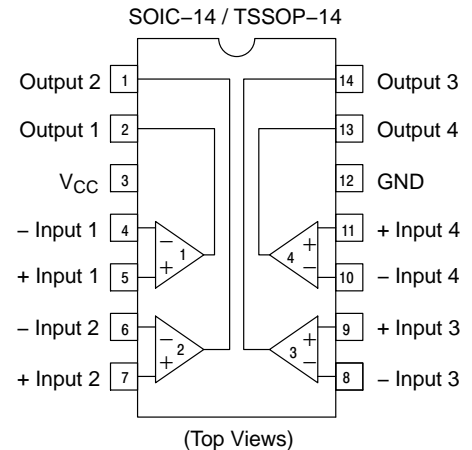
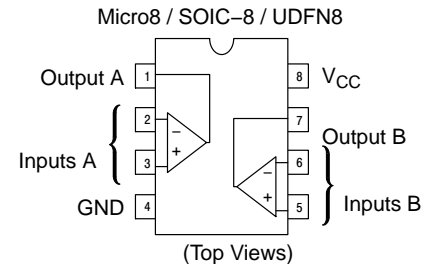
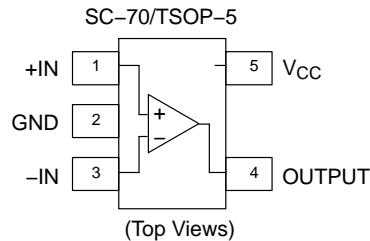
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

**TSSOP-14  
CASE 948G**



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

## PACKAGE PINOUTS



# LMV331, NCV331, LMV393, LMV339

## MAXIMUM RATINGS

| Symbol           | Rating   | Value                   | Unit |
|------------------|--|-------------------------|------|
| V <sub>S</sub>   | Voltage on any Pin (referred to V <sup>-</sup> pin)                              | 5.5                     | V    |
| V <sub>IDR</sub> | Input Differential Voltage Range   | ±Supply Voltage         | V    |
| T <sub>J</sub>   | Maximum Junction Temperature   | 150                     | °C   |
| T <sub>A</sub>   | Operating Ambient Temperature Range<br>LMV331, LMV393, LMV339<br>NCV331 (Note 3) | -40 to 85<br>-40 to 125 | °C   |
| T <sub>stg</sub> | Storage Temperature Range  | -65 to 150              | °C   |
| T <sub>L</sub>   | Mounting Temperature (Infrared or Convection (1/16" From Case for 30 Seconds))   | 260                     | °C   |
| V <sub>ESD</sub> | ESD Tolerance (Note 1)<br>Machine Model<br>Human Body Model                      | 100<br>1000             | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol          | Parameter   | Value   | Unit |
|-----------------|---|---|------|
| V <sub>CC</sub> | Supply Voltage Temperature Range (Note 2)   | 2.7 to 5.0                                    | V    |
| θ <sub>JA</sub> | Thermal Resistance<br>SC-70<br>TSOP-5<br>Micro8<br>SOIC-8<br>UDFN8<br>SOIC-14<br>TSSOP-14 | 280<br>333<br>238<br>212<br>350<br>156<br>190 | °C/W |

- Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC board.
- NCV prefix is qualified for automotive usage.

## LMV331, NCV331, LMV393, LMV339

**2.7 V DC ELECTRICAL CHARACTERISTICS** (All limits are guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = 1.35\text{ V}$  unless otherwise noted.)

| Parameter                          | Symbol                               | Condition                   | Min | Typ                   | Max                      | Unit                         |
|------------------------------------|--------------------------------------|-----------------------------|-----|-----------------------|--------------------------|------------------------------|
| Input Offset Voltage               | $V_{IO}$                             |                             |     | 1.7                   | 9                        | mV                           |
| Input Offset Voltage Average Drift | $T_C V_{IO}$                         |                             |     | 5                     |                          | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current (Note 4)        | $I_B$                                |                             |     | < 1                   |                          | nA                           |
| Input Offset Current (Note 4)      | $I_{IO}$                             |                             |     | < 1                   |                          | nA                           |
| Input Voltage Range                | $V_{CM}$                             |                             |     | 0 to 2                |                          | V                            |
| Saturation Voltage                 | $V_{SAT}$                            | $I_{SINK} \leq 1\text{ mA}$ |     | 120                   |                          | mV                           |
| Output Sink Current                | $I_O$                                | $V_O \leq 1.5\text{ V}$     | 5   | 23                    |                          | mA                           |
| Supply Current                     | $I_{CC}$                             |                             |     | 40<br>40<br>70<br>140 | 100<br>100<br>140<br>200 | $\mu\text{A}$                |
|                                    | LMV331<br>NCV331<br>LMV393<br>LMV339 |                             |     |                       |                          |                              |

**2.7 V AC ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{ V}$ ,  $R_L = 5.1\text{ k}\Omega$ ,  $V^- = 0\text{ V}$  unless otherwise noted.)

| Parameter                       | Symbol    | Condition   | Min | Typ         | Max | Unit |
|---------------------------------|-----------|---|-----|-------------|-----|------|
| Propagation Delay – High to Low | $t_{PHL}$ | Input Overdrive = 10 mV<br>Input Overdrive = 100 mV |     | 1000<br>500 |     | ns   |
| Propagation Delay – Low to High | $t_{PLH}$ | Input Overdrive = 10 mV<br>Input Overdrive = 100 mV |     | 800<br>200  |     | ns   |

4. Guaranteed by design and/or characterization.

## LMV331, NCV331, LMV393, LMV339

**5.0 V DC ELECTRICAL CHARACTERISTICS** (All limits are guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = 2.5\text{ V}$  unless otherwise noted. Limits over temperature are guaranteed by design and/or characterization.)

| Parameter                          | Symbol    | Condition (Note 6)  | Min | Typ      | Max        | Unit                         |
|------------------------------------|-----------|---|-----|----------|------------|------------------------------|
| Input Offset Voltage               | $V_{IO}$  | $T_A = T_{LO}$ to $T_{HIGH}$                              |     | 1.7      | 9          | mV                           |
| Input Offset Voltage Average Drift |           | $T_A = T_{LO}$ to $T_{HIGH}$                              |     | 5        |            | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current (Note 5)        | $I_B$     | $T_A = T_{LO}$ to $T_{HIGH}$                              |     | < 1      |            | nA                           |
| Input Offset Current (Note 5)      | $I_{IO}$  | $T_A = T_{LO}$ to $T_{HIGH}$                              |     | < 1      |            | nA                           |
| Input Voltage Range                | $V_{CM}$  |   |     | 0 to 4.2 |            | V                            |
| Voltage Gain (Note 5)              | $A_V$     |   | 20  | 50       |            | V/mV                         |
| Saturation Voltage                 | $V_{SAT}$ | $I_{SINK} = 10\text{ mA}$<br>$T_A = T_{LO}$ to $T_{HIGH}$ |     | 200      | 400<br>700 | mV                           |
| Output Sink Current                | $I_O$     | $V_O \leq 1.5\text{ V}$                                   | 10  | 84       |            | mA                           |
| Supply Current LMV331              | $I_{CC}$  | $T_A = T_{LO}$ to $T_{HIGH}$                              |     | 60       | 120<br>150 | $\mu\text{A}$                |
| Supply Current LMV393              | $I_{CC}$  | $T_A = T_{LO}$ to $T_{HIGH}$                              |     | 100      | 200<br>250 | $\mu\text{A}$                |
| Supply Current LMV339              | $I_{CC}$  | $T_A = T_{LO}$ to $T_{HIGH}$                              |     | 170      | 300<br>350 | $\mu\text{A}$                |
| Output Leakage Current (Note 5)    |           | $T_A = T_{LO}$ to $T_{HIGH}$                              |     | 0.003    | 1          | $\mu\text{A}$                |

**5.0 V AC ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $R_L = 5.1\text{ k}\Omega$ ,  $V^- = 0\text{ V}$  unless otherwise noted.)

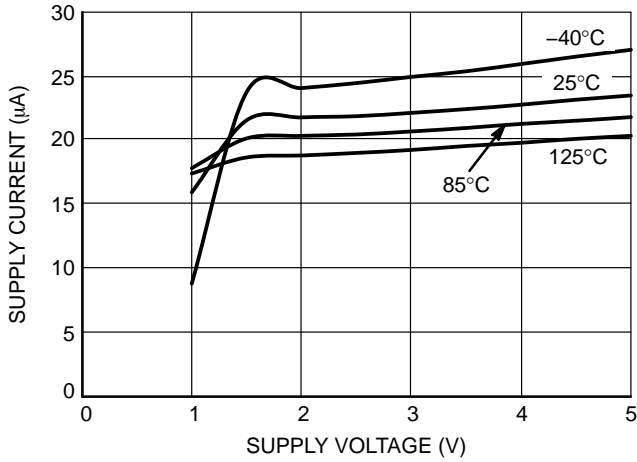
| Parameter                       | Symbol    | Condition   | Min | Typ         | Max | Unit |
|---------------------------------|-----------|---|-----|-------------|-----|------|
| Propagation Delay – High to Low | $t_{PHL}$ | Input Overdrive = 10 mV<br>Input Overdrive = 100 mV |     | 1500<br>900 |     | ns   |
| Propagation Delay – Low to High | $t_{PLH}$ | Input Overdrive = 10 mV<br>Input Overdrive = 100 mV |     | 800<br>200  |     | ns   |

5. Guaranteed by design and/or characterization.
6. For LMV331, LMV393, LMV339:  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$   
For NCV331:  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$

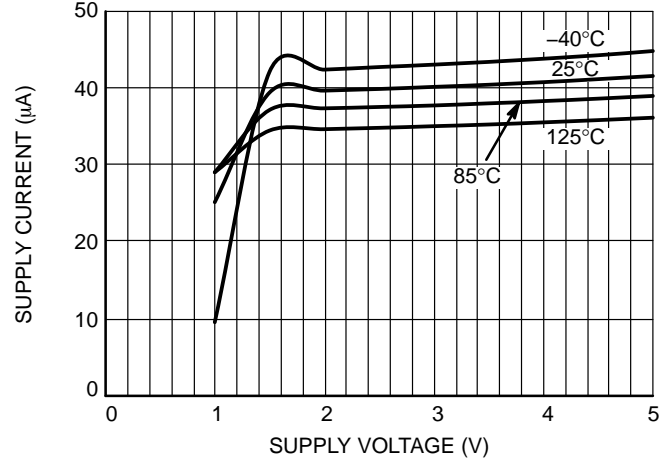
# LMV331, NCV331, LMV393, LMV339

## TYPICAL CHARACTERISTICS

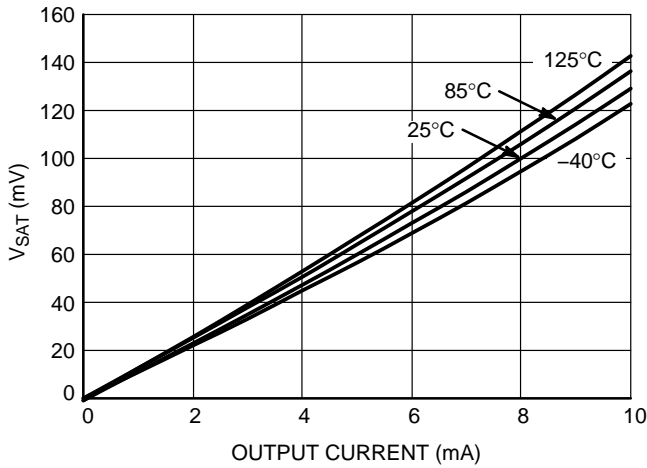
( $V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 5\text{ k}\Omega$  unless otherwise specified)



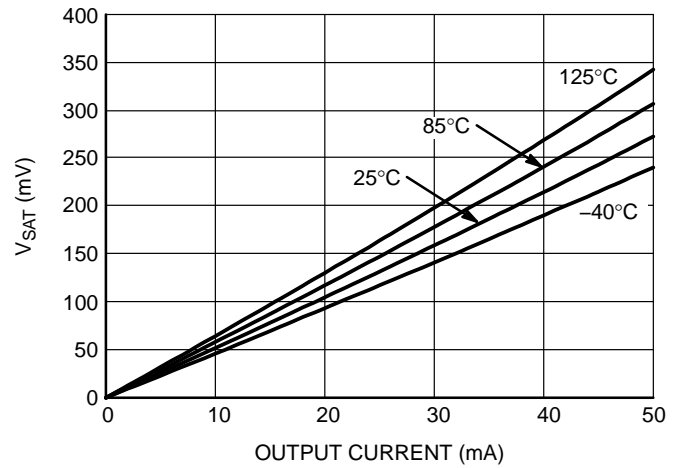
**Figure 3. Supply Current vs. Supply Voltage (Output High)**



**Figure 4. Supply Current vs. Supply Voltage (Output Low)**



**Figure 5.  $V_{SAT}$  vs. Output Current at  $V_{CC} = 2.7\text{ V}$**



**Figure 6.  $V_{SAT}$  vs. Output Current at  $V_{CC} = 5.0\text{ V}$**

# LMV331, NCV331, LMV393, LMV339

## NEGATIVE TRANSITION INPUT – $V_{CC} = 2.7\text{ V}$

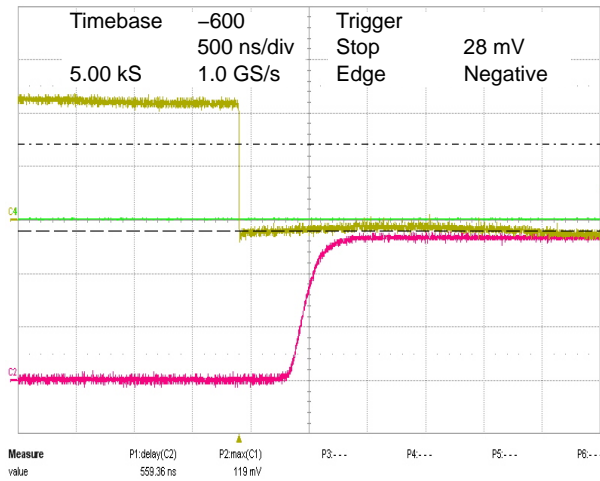


Figure 7. 10 mV Overdrive

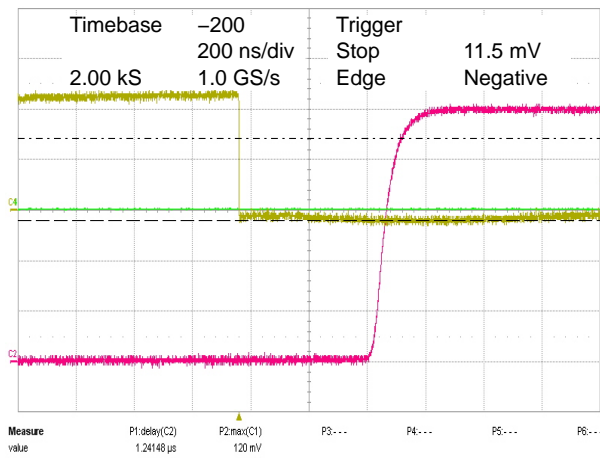


Figure 8. 20 mV Overdrive

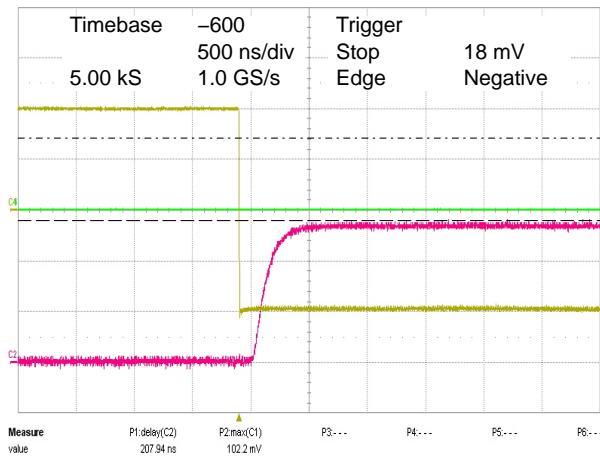


Figure 9. 100 mV Overdrive

# LMV331, NCV331, LMV393, LMV339

## POSITIVE TRANSITION INPUT - $V_{CC} = 2.7\text{ V}$

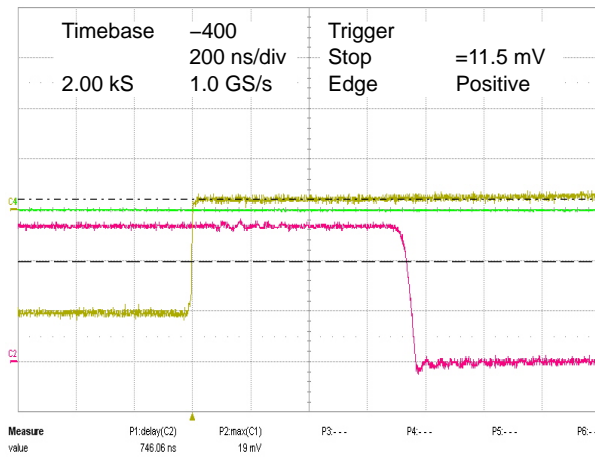


Figure 10. 10 mV Overdrive

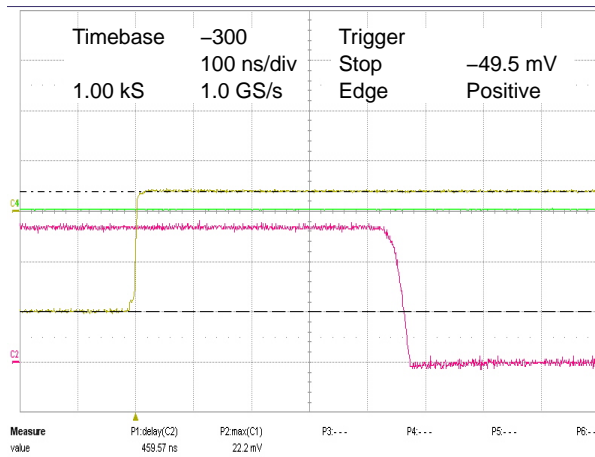


Figure 11. 20 mV Overdrive

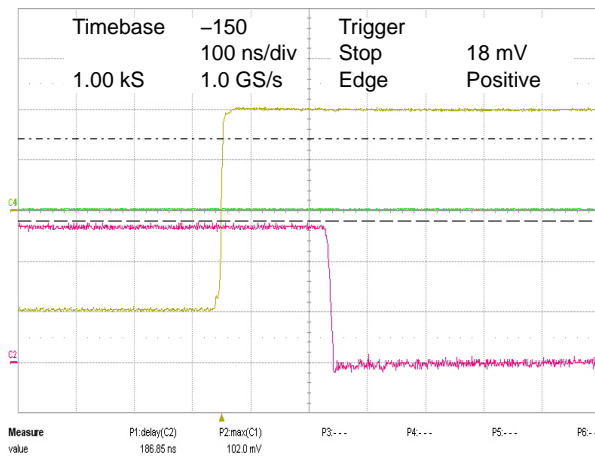


Figure 12. 100 mV Overdrive



# LMV331, NCV331, LMV393, LMV339

NEGATIVE TRANSITION INPUT –  $V_{CC} = 5.0\text{ V}$

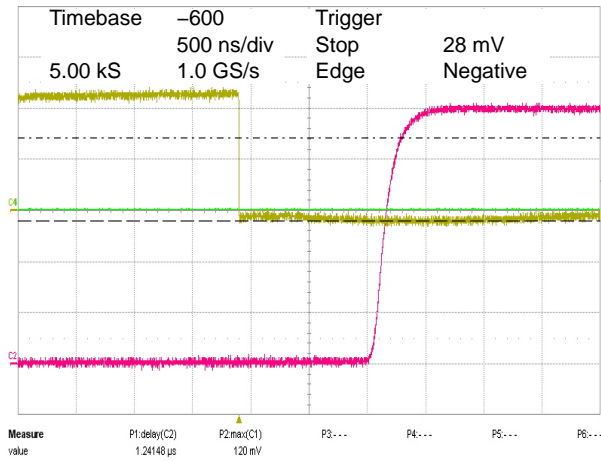


Figure 13. 10 mV Overdrive

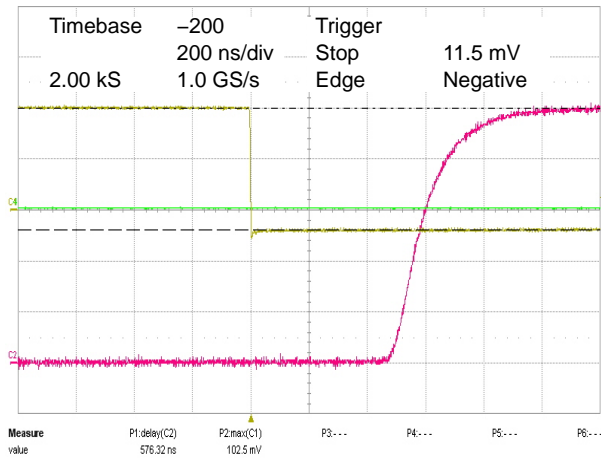


Figure 14. 20 mV Overdrive

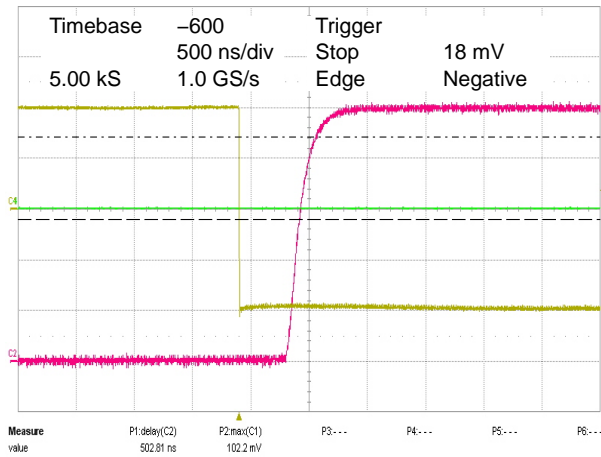


Figure 15. 100 mV Overdrive

# LMV331, NCV331, LMV393, LMV339

## POSITIVE TRANSITION INPUT – $V_{CC} = 5.0\text{ V}$

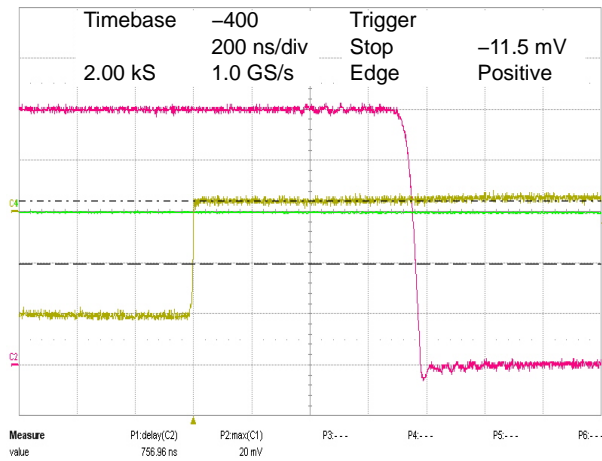


Figure 16. 10 mV Overdrive

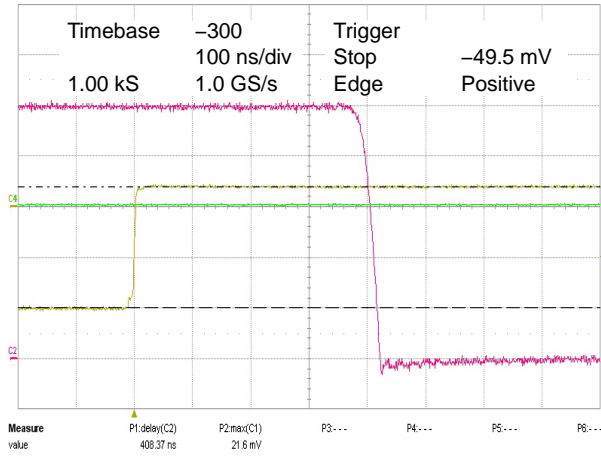


Figure 17. 20 mV Overdrive

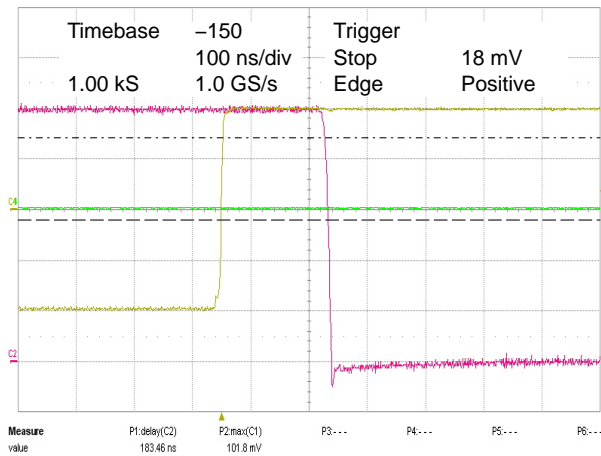


Figure 18. 100 mV Overdrive

APPLICATION CIRCUITS

Basic Comparator Operation

The basic operation of a comparator is to compare two input voltage signals, and produce a digital output signal by determining which input signal is higher. If the voltage on the non-inverting input is higher, then the internal output transistor is off and the output will be high. If the voltage on the inverting input is higher, then the output transistor will be on and the output will be low. The LMV331/393/339 has an open-drain output stage, so a pull-up resistor to a positive supply voltage is required for the output to switch properly.

The size of the pull-up resistor is recommended to be between 1 kΩ and 10 kΩ. This range of values will balance two key factors; i.e., power dissipation and drive capability for interface circuitry.

Figure 19 illustrates the basic operation of a comparator and assumes dual supplies. The comparator compares the input voltage ( $V_{IN}$ ) on the non-inverting input to the reference voltage ( $V_{REF}$ ) on the inverting input. If  $V_{IN}$  is less than  $V_{REF}$ , the output voltage ( $V_O$ ) will be low. If  $V_{IN}$  is greater than  $V_{REF}$ , then  $V_O$  will be high.

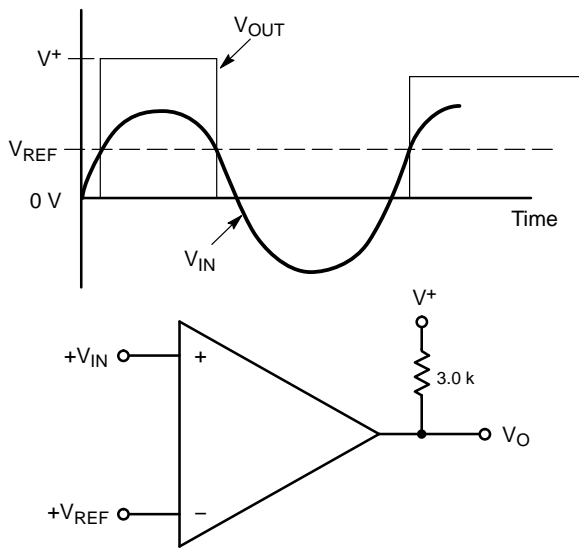


Figure 19.

Comparators and Stability

A common problem with comparators is oscillation due to their high gain. The basic comparator configuration in Figure 19 may oscillate if the differential voltage between the input pins is close to the device's offset voltage. This can happen if the input signal is moving slowly through the comparator's switching threshold or if unused channels are connected to the same potential for termination of unused channels. One way to eliminate output oscillations or 'chatter' is to include external hysteresis in the circuit design.

Inverting Configuration with Hysteresis

An inverting comparator with hysteresis is shown in Figure 20.

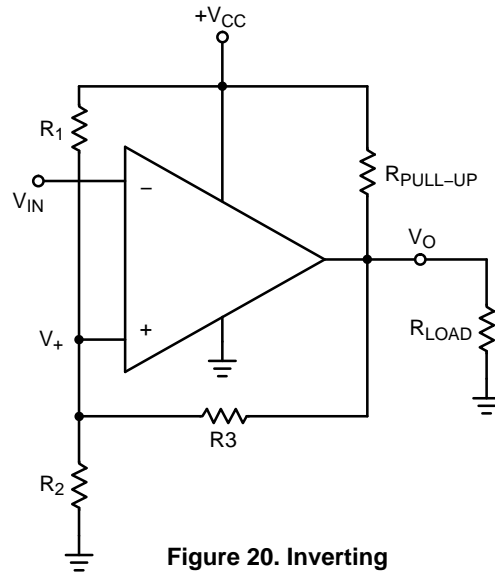


Figure 20. Inverting Comparator with Hysteresis

When  $V_{IN}$  is less than the voltage at the non-inverting node,  $V_+$ , the output voltage will be high. When  $V_{IN}$  is greater than the voltage at  $V_+$ , then the output will be low. The hysteresis band (Figure 21) created from the resistor network is defined as:

$$\Delta V_+ = V_{T1} - V_{T2}$$

where  $V_{T1}$  and  $V_{T2}$  are the lower and upper trip points, respectively.

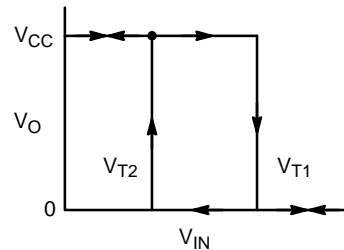


Figure 21.

$V_{T1}$  is calculated by assuming that the output of the comparator is pulled up to supply when high. The resistances  $R_1$  and  $R_3$  can be viewed as being in parallel which is in series with  $R_2$  (Figure 22). Therefore  $V_{T1}$  is:

$$V_{T1} = \frac{V_{CC} R_2}{(R_1 \parallel R_3) + R_2}$$

$V_{T2}$  is calculated by assuming that the output of the comparator is at ground potential when low. The resistances  $R_2$  and  $R_3$  can be viewed as being in parallel which is in series with  $R_1$  (Figure 23). Therefore  $V_{T2}$  is:

$$V_{T2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)}$$

# LMV331, NCV331, LMV393, LMV339

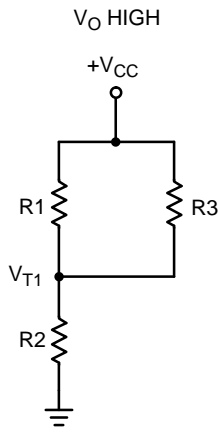


Figure 22.

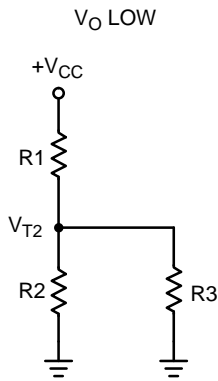


Figure 23.

When  $V_{IN}$  is much less than the voltage at the inverting input ( $V_{REF}$ ), then the output is low.  $R_2$  can then be viewed as being connected to ground (Figure 26). To calculate the voltage required at  $V_{IN}$  to trip the comparator high, the following equation is used:

$$V_{in1} = \frac{V_{ref} (R_1 + R_2)}{R_2}$$

When the output is high,  $V_{IN}$  must be less than or equal to  $V_{REF}$  ( $V_{IN} \leq V_{REF}$ ) before the output will be low again (Figure 27). The following equation is used to calculate the voltage at  $V_{IN}$  to switch the output back to the low state:

$$V_{in2} = \frac{V_{ref} (R_1 + R_2) - V_{CC} R_1}{R_2}$$

## Non-inverting Configuration with Hysteresis

A non-inverting comparator is shown in Figure 24.

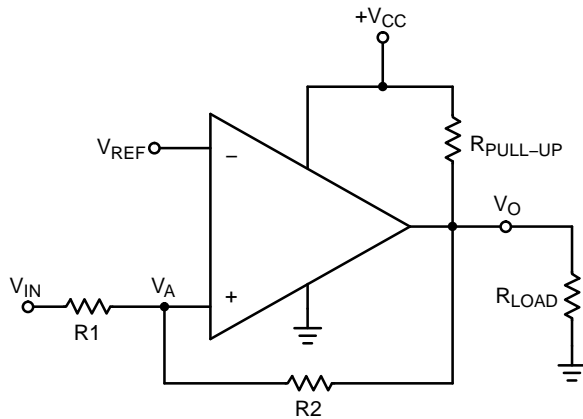


Figure 24.

The hysteresis band (Figure 25) of the non-inverting configuration is defined as follows:

$$\Delta V_{in} = V_{CC} R_1 / R_2$$

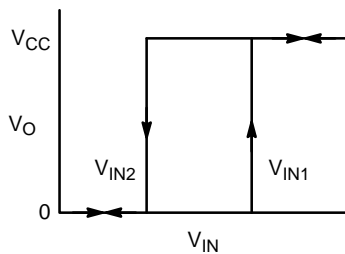


Figure 25.

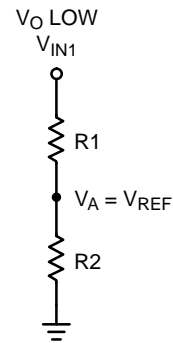


Figure 26.

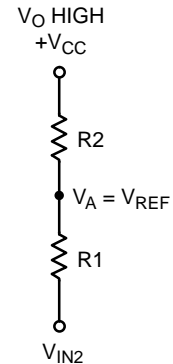


Figure 27.

## Termination of Unused Inputs

Proper termination of unused inputs is a good practice to keep the output from ‘chattering.’ For example, if one channel of a dual or quad package is not being used, then the inputs must be connected to a defined state. The recommended connections would be to tie one input to  $V_{CC}$  and the other input to ground.

## LMV331, NCV331, LMV393, LMV339

### ORDERING INFORMATION

| Order Number | Number of Channels | Specific Device Marking | Package Type          | Shipping†          |
|--------------|--------------------|-------------------------|-----------------------|--------------------|
| LMV331SQ3T2G | Single             | CCA                     | SC-70<br>(Pb-Free)    | 3000 / Tape & Reel |
| LMV331SN3T1G | Single             | 3CA                     | TSOP-5<br>(Pb-Free)   | 3000 / Tape & Reel |
| NCV331SN3T1G | Single             | 3CA                     | TSOP-5<br>(Pb-Free)   | 3000 / Tape & Reel |
| LMV393DMR2G  | Dual               | V393                    | Micro8<br>(Pb-Free)   | 4000 / Tape & Reel |
| LMV393DR2G   | Dual               | V393                    | SOIC-8<br>(Pb-Free)   | 2500 / Tape & Reel |
| LMV393MUTAG  | Dual               | CA                      | UDFN8<br>(Pb-Free)    | 3000 / Tape & Reel |
| LMV339DR2G   | Quad               | LMV339                  | SOIC-14<br>(Pb-Free)  | 2500 / Tape & Reel |
| LMV339DTBR2G | Quad               | LMV<br>339              | TSSOP-14<br>(Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*Contact factory.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



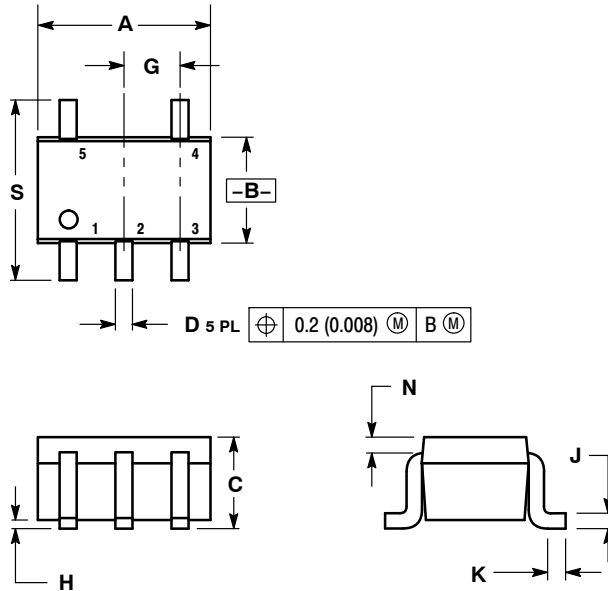
### SC-88A (SC-70-5/SOT-353)

#### CASE 419A-02

#### ISSUE L

SCALE 2:1

DATE 17 JAN 2013

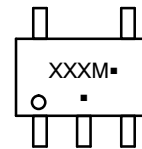


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES    |       | MILLIMETERS |      |
|-----|-----------|-------|-------------|------|
|     | MIN       | MAX   | MIN         | MAX  |
| A   | 0.071     | 0.087 | 1.80        | 2.20 |
| B   | 0.045     | 0.053 | 1.15        | 1.35 |
| C   | 0.031     | 0.043 | 0.80        | 1.10 |
| D   | 0.004     | 0.012 | 0.10        | 0.30 |
| G   | 0.026 BSC |       | 0.65 BSC    |      |
| H   | ---       | 0.004 | ---         | 0.10 |
| J   | 0.004     | 0.010 | 0.10        | 0.25 |
| K   | 0.004     | 0.012 | 0.10        | 0.30 |
| N   | 0.008 REF |       | 0.20 REF    |      |
| S   | 0.079     | 0.087 | 2.00        | 2.20 |

### GENERIC MARKING DIAGRAM\*

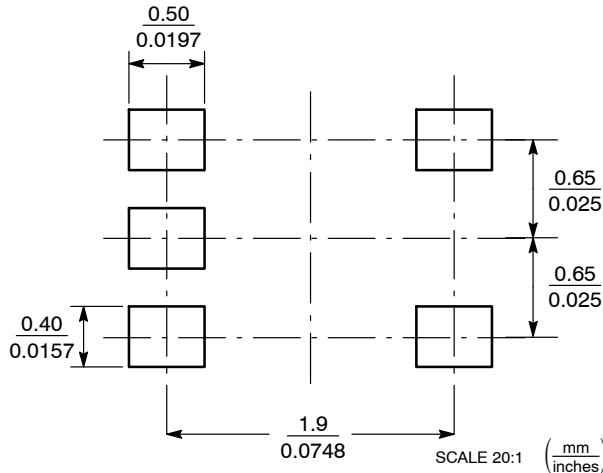


- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDER FOOTPRINT



STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

STYLE 2:  
PIN 1. ANODE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. CATHODE

STYLE 3:  
PIN 1. ANODE 1  
2. N/C  
3. ANODE 2  
4. CATHODE 2  
5. CATHODE 1

STYLE 4:  
PIN 1. SOURCE 1  
2. DRAIN 1/2  
3. SOURCE 1  
4. GATE 1  
5. GATE 2

STYLE 5:  
PIN 1. CATHODE  
2. COMMON ANODE  
3. CATHODE 2  
4. CATHODE 3  
5. CATHODE 4

STYLE 6:  
PIN 1. EMITTER 2  
2. BASE 2  
3. EMITTER 1  
4. COLLECTOR  
5. COLLECTOR 2/BASE 1

STYLE 7:  
PIN 1. BASE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

STYLE 8:  
PIN 1. CATHODE  
2. COLLECTOR  
3. N/C  
4. BASE  
5. EMITTER

STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. ANODE

|                         |                                  |  |
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| <b>NEW STANDARD:</b>    |                                  |  |
| <b>DESCRIPTION:</b>     | <b>SC-88A (SC-70-5/SOT-353)</b>  | <b>PAGE 1 OF 2</b>   |



| ISSUE | REVISION   | DATE        |
|-------|--|-------------|
| C     | CONVERTED FROM PAPER DOCUMENT TO ELECTRONIC. REQ. BY N LAFEBRE.  | 20 JUN 1998 |
| D     | CONVERTED FROM MOTOROLA TO ON SEMICONDUCTOR. ADDED STYLE 5. REQ. BY E. KIM.                                  | 24 JUL 2000 |
| E     | ADDED STYLES 6 & 7. REQ. BY S. BACHMAN.  | 03 AUG 2000 |
| F     | DELETED DIMENSION V, WAS 0.3-0.44MM/0.012-0.016IN. REQ. BY G. KWONG.   | 14 JUN 2001 |
| G     | ADDED STYLE 8, REQ. BY S. CHANG; ADDED STYLE 9, REQ. BY S. BACHMAN; ADDED NOTE 4, REQ. BY S. RIGGS           | 25 JUN 2003 |
| H     | CHANGED STYLE 6. REQ. BY C. LIM  | 28 APR 2005 |
| J     | CHANGED TITLE DESCRIPTION. REQ. BY B. LOFTS.   | 31 AUG 2005 |
| K     | CORRECTED TITLE AND DESCRIPTION TO SC-88A (SC-70-5/SOT-353). CORRECTED MARKING DIAGRAM. REQ. BY D. TRUHITTE. | 13 JUL 2010 |
| L     | ADDED SOLDER FOOTPRINT. REQ. BY I. MARIANO.  | 17 JAN 2013 |
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

### TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 2.85        | 3.15 |
| B   | 1.35        | 1.65 |
| C   | 0.90        | 1.10 |
| D   | 0.25        | 0.50 |
| G   | 0.95 BSC    |      |
| H   | 0.01        | 0.10 |
| J   | 0.10        | 0.26 |
| K   | 0.20        | 0.60 |
| M   | 0°          | 10°  |
| S   | 2.50        | 3.00 |

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code    XXX = Specific Device Code  
 A = Assembly Location        M = Date Code  
 Y = Year                            ■ = Pb-Free Package  
 W = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

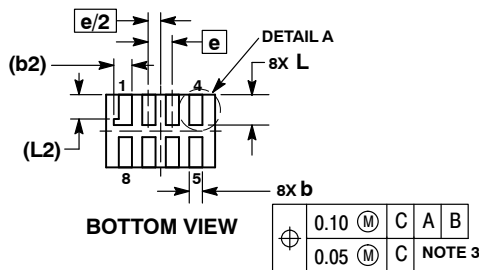
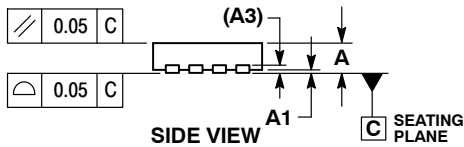
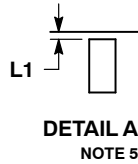
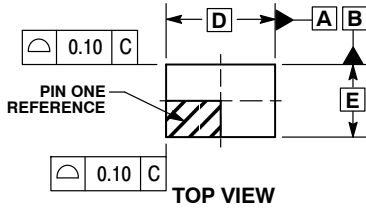
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SCALE 4:1

UDFN8 1.8x1.2, 0.4P  
CASE 517AJ-01  
ISSUE O

DATE 08 NOV 2006

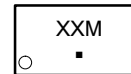


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.45        | 0.55 |
| A1  | 0.00        | 0.05 |
| A3  | 0.127       | REF  |
| b   | 0.15        | 0.25 |
| b2  | 0.30        | REF  |
| D   | 1.80        | BSC  |
| E   | 1.20        | BSC  |
| e   | 0.40        | BSC  |
| L   | 0.45        | 0.55 |
| L1  | 0.00        | 0.03 |
| L2  | 0.40        | REF  |

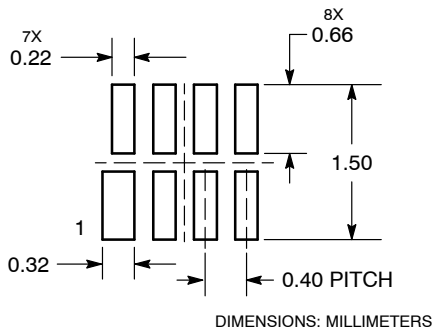
**GENERIC MARKING DIAGRAM\***



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**MOUNTING FOOTPRINT  
SOLDERMASK DEFINED**



|                         |                            |  |
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

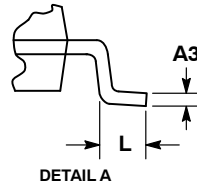
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SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

### Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



TOP VIEW

NOTE 3



SIDE VIEW

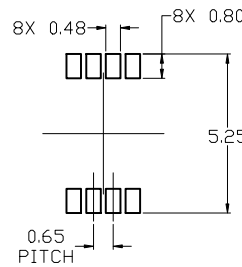


END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀ 0.08 (0.003) M C B S A S



RECOMMENDED MOUNTING FOOTPRINT

| DIM                  | MILLIMETERS |      |      |
|----------------------|-------------|------|------|
|                      | MIN.        | NOM. | MAX. |
| A                    | ---         | ---  | 1.10 |
| A1                   | 0.05        | 0.08 | 0.15 |
| <i>b</i>             | 0.25        | 0.33 | 0.40 |
| <i>c</i>             | 0.13        | 0.18 | 0.23 |
| <i>D</i>             | 2.90        | 3.00 | 3.10 |
| <i>E</i>             | 2.90        | 3.00 | 3.10 |
| <i>e</i>             | 0.65 BSC    |      |      |
| <i>H<sub>E</sub></i> | 4.75        | 4.90 | 5.05 |
| <i>L</i>             | 0.40        | 0.55 | 0.70 |

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT**



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