DATA SHEET

SPFD54126B

528-channel 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

Preliminary

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Version 0.2

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528-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

1. GENERAL DESCRIPTION

The SPF54126B, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 176xRGBx220 in resolution which can be achieved by the designated RAM for graphic data. The 528-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter. The source driver of SPFD54126B adopts OP-AMP structure to enhance display quality and it cooperates with advanced circuitry techniques to reduce power consumption.

The SPFD54126B is able to operate with low IO interface power supply up to 1.6V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and common driver.

The built-in timing controller in SPFD54126B can support several interfaces for the diverse request of medium or small size portable display. SPFD54126B provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and 9-bit serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the SPFD54126B incorporates 6, 16, and 18-bit RGB interfaces for picture movement display. The SPFD54126B also supports a function to display eight colors and a standby mode for power control consideration.

2. FEATURE

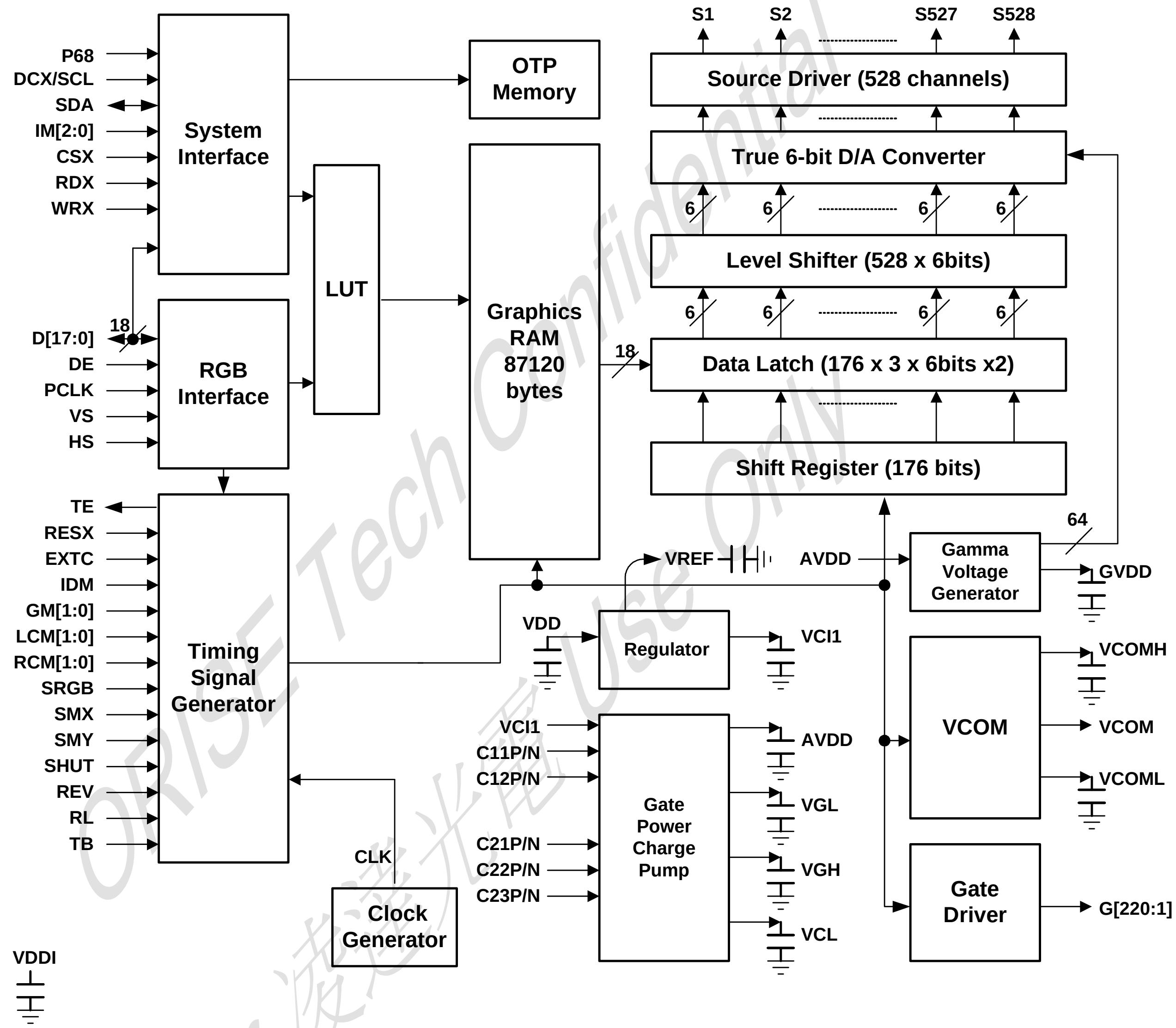
- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 176xRGBx220, incorporating a 528-channel source driver and a 220-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- 528-channel source driver adopts OP-AMP structure
- Built-in 87120 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - Logic power supply voltage (VDD): 2.6 ~ 3.5 V
  - I/O interface supply voltage (VDDI): 1.6 ~ 3.6 V
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption OP-AMP structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level : 2 times (x2) of Vci1
  - Gate driver voltage level (VGH, VGL) up to 6 times (x6) and minus 5 times (x-5) Vci1
- Built-in internal oscillator and hardware reset
- Built–in One-Time-Programming (OTP) function for VCOM amplitude and VcomH voltage adjustment.
- Built-in separate three-gamma curves (RGB) controller to fine tune display quality.

3. ORDERING INFORMATION

Product Number	Package Type
SPFD54126B-C	Chip Form With Gold Bump

4. BLOCK DIAGRAM

4.1. Block Function



4.1.1. System Interface

The SPFD54126B supports three high-speed system interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. 68-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
3. 3-pin 9-bits Serial Peripheral Interface (SPI).

The SPFD54126B has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the SPFD54126B executes the 1st read operation. Thus, valid data can be read out after the SPFD54126B executes the 2nd read operation.

4.1.2. External Display Interface

The SPFD54126B supports external RGB interface for picture movement display.

The SPFD54126B allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

4.1.3. Address Counter (AC)

SPFD54126B features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

4.1.4. Graphics RAM (GRAM)

SPFD54126B features a 87120-byte (176 x 220x 18/8) Graphic RAM (GRAM).

4.1.5. Grayscale Voltage Generating Circuit

SPFD54126B has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register. For details, see the "γ-Correction Function" section.

4.1.6. Timing Controller

SPFD54126B has a timing controller which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

4.1.7. Oscillator (OSC)

The SPFD54126B also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption. See "Oscillator" for details.

4.1.8. Source Driver Circuit

SPFD54126B consists of a 528-output source driver circuit (S1 ~ S528). Data in the GRAM are latched when the 528th bit data is input. The latched data controls the source driver and generates a drive waveform.

4.1.9. Gate Driver Circuit

SPFD54126B consists of a 220-output gate driver circuit (G1~G220). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

4.1.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels AVDD, VGH, VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>Pin No.</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="5">System Configuration Input Signal</td></tr>
<tr><td>P68, IM2~0</td><td>4</td><td>I</td><td>DGND/ VDDI</td><td>Select system interface mode.
<table>
<tr><th>P68</th><th>IM2</th><th>IM1</th><th>IM0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>-</td><td>-</td><td>3-Pin Serial interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8080 MCU 8-bits Parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>8080 MCU 16-bits Parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>8080 MCU 9-bits Parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8080 MCU 18-bits Parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>-</td><td>-</td><td>3-Pin Serial interface</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>6800 MCU 8-bits Parallel interface</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>6800 MCU 16-bits Parallel interface</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>6800 MCU 9-bits Parallel interface</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>6800 MCU 18-bits Parallel interface</td></tr>
</table>
Must connect to the GND or VDDI level when not used.</td></tr>
<tr><td>RESX</td><td>1</td><td>I</td><td>MPU or
external
RC circuit</td><td>Reset pin. This is an active low signal.</td></tr>
<tr><td>EXTC</td><td>1</td><td>I</td><td>DGND/ VDDI</td><td>Extend command set access
Low: Extend command set is not accessible.
High: Extend command set is accessible.
If this is not used. Open it (This pin is internally pull low).</td></tr>
<tr><td>GM1~0</td><td>2</td><td>I</td><td>DGND/ VDDI</td><td>Resolution selection:
<table>
<tr><th>GM1</th><th>GM0</th><th>Resolution</th></tr>
<tr><td>0</td><td>0</td><td>176*RGB*220</td></tr>
<tr><td>0</td><td>1</td><td>176*RGB*176</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>176*RGB*132</td></tr>
</table></td></tr>
<tr><td>RCM1~0</td><td>2</td><td>I</td><td>DGND/ VDDI</td><td>Interface selection:
<table>
<tr><th>RCM1</th><th>RCM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>MCU Interface</td></tr>
<tr><td>0</td><td>1</td><td>MCU Interface</td></tr>
<tr><td>1</td><td>0</td><td>RGB Interface</td></tr>
<tr><td>1</td><td>1</td><td>RGB Interface</td></tr>
</table></td></tr>
<tr><td>IDM</td><td>1</td><td>I</td><td>MCU</td><td>In RGB interface mode:
(a) Low: Normal Display.
(b) High: Idle Mode (8-color mode).
This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>LCM</td><td>2</td><td>I</td><td>DGND/ VDDI</td><td>Liquid Crystal Type selection:
<table>
<tr><th>LCM1</th><th>LCM0</th><th>LC type selection</th></tr>
<tr><td>0</td><td>0</td><td>Normally black type1</td></tr>
<tr><td>0</td><td>1</td><td>Normally white type1</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Signal</th><th>Pin No.</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td></td><td><table><tr><td>1</td><td>0</td><td>Normally black type2</td></tr><tr><td>1</td><td>1</td><td>Normally white type2</td></tr></table></td></tr>
<tr><td>SRGB</td><td>1</td><td>I</td><td>DGND/ VDDI</td><td>RGB arrangement selection:<table><tr><th>RGB</th><th>SRGB</th><th>RGB filter order for CF default setting</th></tr><tr><td>0</td><td>0</td><td>S1, S2, S3 fit ‘R’, ‘G’, ‘B</td></tr><tr><td>0</td><td>1</td><td>S1, S2, S3 fit ‘B’, ‘G’, ‘R</td></tr><tr><td>1</td><td>0</td><td>S1, S2, S3 fit ‘B’, ‘G’, ‘R</td></tr><tr><td>1</td><td>1</td><td>S1, S2, S3 fit ‘R’, ‘G’, ‘B</td></tr></table>The RGB is the D4 for Command 36H</td></tr>
<tr><td>SHUT</td><td>1</td><td>I</td><td>DGND/ VDDI</td><td>Display on/off selection when RGB mode is selected.
(a) Low: Display On.
(b) High: Display Off.
This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>REV</td><td>1</td><td>I</td><td>DGND/ VDDI</td><td>Data reverse for source driver selection when RGB mode is selected.
(a) Low: Reverse Off.
(b) High: Reserve On.
This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>SMX</td><td>1</td><td>I</td><td>DGND/ VDDI</td><td>Source driver output direction selection:<table><tr><th>SMX</th><th>Source output direction</th></tr><tr><td>0</td><td>S1 => S528</td></tr><tr><td>1</td><td>S528=>S1</td></tr></table></td></tr>
<tr><td>SMY</td><td>1</td><td>I</td><td>DGND/ VDDI</td><td>Gate driver output direction selection:<table><tr><th>SMY</th><th>GM=”00”</th><th>GM=”01”</th><th>GM=”11”</th></tr><tr><td>0</td><td>G1 =>G220</td><td>G1=>G176</td><td>G1=>G132</td></tr><tr><td>1</td><td>G220=>G1</td><td>G176=>G1</td><td>G132=>G1</td></tr></table></td></tr>
<tr><td>RL</td><td>1</td><td>I</td><td>DGND/ VDDI</td><td>Source driver output direction selection:<table><tr><th>SMX</th><th>RL</th><th>Source output direction</th></tr><tr><td>0</td><td>0</td><td>S1 => S528</td></tr><tr><td>0</td><td>1</td><td>S528 => S1</td></tr><tr><td>1</td><td>0</td><td>S528 => S1</td></tr><tr><td>1</td><td>1</td><td>S1 => S528</td></tr></table>This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>TB</td><td>1</td><td>I</td><td>DGND/ VDDI</td><td>Gate driver output direction selection:<table><tr><th>SMY</th><th>TB</th><th>GM=”00”</th><th>GM=”01”</th><th>GM=”11”</th></tr><tr><td>0</td><td>0</td><td>G1 =>G220</td><td>G1=>G176</td><td>G1=>G132</td></tr><tr><td>0</td><td>1</td><td>G220 =>G1</td><td>G176 =>G1</td><td>G132=>G1</td></tr><tr><td>1</td><td>0</td><td>G220 =>G1</td><td>G176 =>G1</td><td>G132=>G1</td></tr><tr><td>1</td><td>1</td><td>G1 =>G220</td><td>G1=>G176</td><td>G1=>G132</td></tr></table>This pin can be only used when RGB mode is selected.</td></tr>
<tr><td colspan="5">Interface input Signals</td></tr>
<tr><td>CSX</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the SPFD54126B is accessible</td></tr>
</table>

Signal	Pin No.	I/O	Connected with	Function
				High: the SPFD54126B is not accessible This pin has can be permanently fixed "Low" in MCU interface mode only.
D/CX (SCL)	1	I	MPU	Display data / Command selection pin in parallel interface Low: Command data High: Display data In SPI I/F, this is used as SCL pin. Must connect to the GND or VDDI level when not used.
WRX (R/WX)	1	I	MPU	(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low. (B) In 68-system interface mode, a write or read control signal can be input via this pin and initializes a write or read operation. Must connect to the GND or VDDI level when not used.
RDX (E)	1	I	MPU	(A) In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low. (B) In 68system interface mode, a strobe signal can be input via this pin and initializes a write or read operation when the signal is low. Must connect to the GND or VDDI level when not in use.
SPI_CSX	1	I	MPU	(A) When RCM [1:0] = '01' Chip select pin for SPI (Low active) (B) When RCM [1:0] = '00' or '1X' This pin is not used, and fix at VDDI or DGND level. If not used, please fix this pin at VDDI or DGND level.
SCL	1	I	MPU	(A) When RCM [1:0] = '01' Serial clock signal pin for SPI (B) When RCM [1:0] = '00' or '1X' This pin is not used, and fix at VDDI or DGND level. If not used, please fix this pin at VDDI or DGND level.
SDA	1	I/O	MPU	(A) When RCM [1:0] = '01' or '1X' Serial input/ output signal in serial I/F mode. The data is input on the rising edge of the SCL signal. The data is output on the falling edge of the SCL signal. (B) When RCM [1:0] = '00' This pin is not used, and fix at VDDI or DGND level. If not used, please fix this pin at VDDI or DGND level.
DB0-DB17	2*18	I/O	MPU	(A) When RCM [1:0] = '1X' (RGB I/F), D[17:0] are used for RGB interface data bus (B) When RCM [1:0] = '00' (MCU I/F), D[17:0] are used to MCU parallel interface data bus In SPI I/F, D0 is used as Serial input/ output signal. In SPI I/F, D[17:1] not used, please fix this pin at VDDI or DGND level. (C) When RCM [1:0] = '01' (MCU I/F), D[17:0] are used for MCU interface data bus In SPI I/F, D[17:0] not used, please fix this pin at VDDI or DGND level.
VS	1	I	MPU	In RGB I/F or VSYNC I/F mode, served as a vertical synchronize signal input Must connect to the VDDI or DGND level when not in use.
HS	1	I	MPU	In RGB I/F mode, served as a horizontal synchronized signal input Must connect to the VDDI or DGND level when not in use.
DE	1	I	MPU	In RGB I/F mode, polarity of DE signal is synchronized with valid graphic data input. High: Valid data on DB17-DB0 Low: Invalid data on DB17-DB0

Signal	Pin No.	I/O	Connected with	Function
				Must connect to the VDDI or DGND level when not in use.
PCLK	1	I	MPU	In RGB I/F mode, served as a pixel clock signal. Must connect to the VDDI or DGND level when not in use.
Charge Pump and Power Supply Signal				
C11P/N, C12P/N C21P/N, C22P/N C23P/N	4/4 4/4 3/3 3/3 3/3	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used.
VCI1	5	O	Stabilizing capacitor	An internal reference voltage level, which is regulated from VDD. The amplitude of VCI1 is from VDD-GND. Place a stabilizing capacitor between GND.
AVDD	6	O	Stabilizing capacitor	Output 2x VCI1 voltage level from the step-up circuit 1. Place a stabilizing capacitor between GND. AVDD = 4.5 ~ 5.5V
VGH	3	O	Stabilizing capacitor	An output voltage from the step-up circuit 2x, 4x ~ 6x of the VCI1 level. Connect with a stabilizing capacitor.
VGL	3	O	Stabilizing capacitor	An output voltage from the step-up circuit –2x, -3x ~ -5x of the VCI1 level. Connect with a stabilizing capacitor.
VCL	3	O	Stabilizing capacitor	An output voltage from the step-up circuit 2, –1x of the VCI1 level. Connect with a stabilizing capacitor.
VCC	5	O	Stabilizing capacitor	Reference voltage for Internal logic block Connect with a stabilizing capacitor
VREF	5	O	Stabilizing capacitor	Reference voltage for power block Connect with a stabilizing capacitor.
GVDD	4	I/O	Stabilizing capacitor	Output source driver grayscale reference voltage level.
Source/Gate Driver and VCOM Signals				
G1~G220	220	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S528	528	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage is output.
VCOM	6	O	TFT panel common electrode	Output a square wave signal with the swing from VcomH - VcomL to the common electrode of TFT panel. The alternating cycle can be set to frame inversion or 1-line inversion.
VcomH	4	O	Stabilizing capacitor	Output the high level of VCOM voltage. Connect with a capacitor to stabilize.
VcomL	4	O	Stabilizing capacitor or open	Output the low level of VCOM voltage. Connect with a capacitor to stabilize.
VDDIO	5	O		VDDI input voltage for control pins using
DGNDO	10	O		DGND input voltage for control pins using
VDD	10	I	Stabilizing capacitor	Power supply Input for analog and booster system
VDDI	8	I	Stabilizing capacitor	Power supply Input for I/O system
DGND	12			Digital ground pin.

Signal	Pin No.	I/O	Connected with	Function
AGND	15			Analog ground pin.
Misc. Signal				
DRV	2	O		Drive signal for the power transistor of the LED booster converter
FB	1	I		LED booster regulator feedback input. Connect feedback resistive divider to GND. FB threshold is 0.6V normal.
TE	1	O	MPU	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is DGND level.
VOTP	2	I		Power supply input for OTP function
PADA0	1	I		This pin is used for glass break detection
PADB0	1	O		This pin is used for glass break detection
PADA1/PADB1 PADA2/PADB2 PADA3/PADB3 PADA4/PADB4	8			This pin is used for chip attachment detection
TEST	18	T		Test pin. If not used, please open this pin.
Dummy	22	D		Dummy pin. If not used, please open this pin.
PREG	1	D		Dummy pin. If not used, please open this pin.
OSC	1	I		External oscillator frequency input pin for oscillator testing If not used, please open this pin.

6. INSTRUCTIONS

6.1. Outline

The SPFD54126B supports 18-bit data bus interface to configure system via accessing command register. When the command register is executed, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with DC/X, WRX, RDX signal for SPFD54126B to recognize the control instruction. And command instruction can be accomplished using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80- or 68-system and SPI)..

6.1.1. System Function Command List and Description

Table 5.1.1 list all the system function command. After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer “RESET TABLE” section). Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTR (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

Table 6.1.1 System Function command List (1)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	ST25	ST24		-
	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	↑	-	GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0		-
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0		-
RDD MADCTR	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTR
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	MX	MY	MV	ML	RGB	D2	D1	D0		-
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	D5	D4	D3	IFPF2	IFPF1	IFPF0		-
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0		-
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0		-
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0		-

“-“: Don’ t care, can be set to VDDI or DGND level

Table 6.1.1 System Function command List (2)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off (normal)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0		-
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0 ≤ XS ≤ 0xAF
	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address end: XS ≤ XE ≤ 0xAF
	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0 ≤ YS ≤ 0xDB
	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address end: YS ≤ YE ≤ 0xDB
	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		Read data
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)	LUT for 4k,65k , 262K color display
	1	↑	1	-	R007	R006	R005	R004	R003	R002	R001	R000		Red tone 0
	1	↑	1	-	:	:	:	:	:	:	:	:		: -
	1	↑	1	-	Ra7	Ra6	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0		Red tone "31"
	1	↑	1	-	G007	G006	G005	G004	G003	G002	G001	G000		Green tone 0
	1	↑	1	-	:	:	:	:	:	:	:	:		: -
	1	↑	1	-	Gb7	Gb6	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0		Green tone "63"
	1	↑	1	-	B007	B006	B005	B004	B003	B002	B001	B000		Blue tone 0
	1	↑	1	-	:	:	:	:	:	:	:	:		: -
	1	↑	1	-	Bc7	Bc6	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0		Blue tone "31"

"-": Don't care, can be set to VDDI or DGND level

Table 6.1.1 System Function command List (3)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address (0,1,2, .., 219)
	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0,1,2, .., 219)
	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
SCRLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		Top fixed area (0,1,2, .., 220)
	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		Vertical scroll area (0,1,2, ..,220)
	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		Bottom fixed area (0,1,2, ..,220)
	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
	1	↑	1	-	0	0	0	0	0	0	0	TELOM		M="0": Mode1, M="1": Mode2
MADCTR	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0		-
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll start address of RAM
	1	↑	1	-	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8		SSA = 0, 1, 2, …, 219
	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1	-	0	0	0	0	0	IFPF2	IFPF1	IFPF0		Interface format
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter
SRGBOFF	0	↑	1	-	1	0	1	0	1	0	1	0	(AAh)	Separate RGB γ function OFF
SRGBON	0	↑	1	-	1	0	1	0	1	0	1	1	(ABh)	Separate RGB γ function ON
VSUNCOFF	0	↑	1	-	1	0	1	0	1	1	0	0	(ACh)	VSYNC interace function OFF
VDUNCON	0	↑	1	-	1	0	1	0	1	1	0	1	(ADh)	VSYNC interace function ON
VSCTRI	0	↑	1	-	1	0	1	0	1	1	1	0	(AEh)	VSYNC interace control
	1	↑	1	-	VSFP3	VSFP2	VSFP1	VSFP0	VSBP3	VSBP2	VSBP1	VSBP0		VS porch setting

"-": Don't care, can be set to VDDI or DGND level

6.1.2. Panel Function Command List and Description

Table 6.1.2 list all the panel function command. Panel function command is only accessible when EXTC is pulled high state (by VDDIO).

Table 6.1.2 Panel Function command List (1)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
RGBCTR	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	Set RGB signal control ICM: RGB data ascess select DP,HSP,VSP:PCLK,HS,VS polarity set
	1	↑	1	-	0	0	0	ICM	DP	EP	HSP	VSP		
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode (Full colors) FP0: Front porch in normal mode BP0: Back porch in normal mode RTN0: Number of clock / one line
	1	↑	1	-	-	-	-	-	FP0 [3]	FP0 [2]	FP0 [1]	FP0 [0]		
	1	↑	1	-					BP0 [3]	BP0 [2]	BP0 [1]	BP0 [0]		
	1	↑	1	-					RTN0 [3]	RTN0 [2]	RTN0 [1]	RTN0 [0]		
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle mode (8-colors) FP1: Front porch in idle mode BP1: Back porch in idle mode RTN1: Number of clock / one line
	1	↑	1	-					FP1 [3]	FP1 [2]	FP1 [1]	FP1 [0]		
	1	↑	1	-					BP1 [3]	BP1 [2]	BP1 [1]	BP1 [0]		
	1	↑	1	-					RTN1 [3]	RTN1 [2]	RTN1 [1]	RTN1 [0]		
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In partial mode + Full colors FP2: Front porch in partial mode BP2: Back porch in partial mode RTN2: Number of clock / one line
	1	↑	1	-					FP2 [3]	FP2 [2]	FP2 [1]	FP2 [0]		
	1	↑	1	-					BP2 [3]	BP2 [2]	BP2 [1]	BP2 [0]		
	1	↑	1	-					RTN2 [3]	RTN2 [2]	RTN2 [1]	RTN2 [0]		
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control NLA, NLB, NLC: set inversion
	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		
RGB PRCTR	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	RGB I/F Blanking porch setting Vertical back porch in RGB mode
	1	↑	1	-	-	-	-	-	VBP [3]	VBP [2]	VBP [1]	VBP [0]		
DISSET5	0	↑	1	-	1	0	1	1	0	1	1	1	(B6h)	Display function setting NO: the amount of non-overlap SDT: set amount of source delay PT: No display area source/ VCOM/ Gate output control EQ: set EQ period
	1	↑	1	-	0	0	NO1	NO0	SDT1	STD0	EQ1	EQ0		
	1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0		

“-“: Don’t care, can be set to VDDI or DGND level

Table 6.1.2 Panel Function Command List (2)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PWCTR1	0	↑	1	-	1	0	1	1	0	0	0	0	(C0h)	Power control setting VRH: Set the GVDD voltage VC : Set the VCI1 voltage Power control setting
	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0		
	1	↑	1		0	0	0	0	0	VC2	VC1	VC0		
PWCTR2	0	↑	1	-	1	0	1	1	0	0	0	1	(C1h)	BT: set AVDD/VCL/ VGH/ VGL voltage
	1	↑	1	-	0	0	0	0	0	BT2	BT1	BT0		
PWCTR3	0	↑	1	-	1	0	1	1	0	0	1	0	(C2h)	n normal mode (Full colors) APA: adjust the operational amplifier DCA: adjust the booster circuit for Idle mode
	1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0		
	1	↑	1	-	0	0	0	0	0	DCA2	DCA1	DCA0		
PWCTR4	0	↑	1	-	1	0	1	1	0	0	1	1	(C3h)	In Idle mode (8-colors) APB: adjust the operational amplifier DCB: adjust the booster circuit for Idle mode l
	1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0		
	1	↑	1	-	0	0	0	0	0	DCB2	DCB1	DCB0		
PWCTR5	0	↑	1	-	1	0	1	1	0	1	0	0	(C4h)	In partial mode + Full colors APC: adjust the operational amplifier DCC: adjust the booster circuit for Idle mode
	1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0		
	1	↑	1	-	0	0	0	0	0	DCC2	DCC1	DCC0		
VMCTR1	0	↑	1	-	1	0	1	1	0	1	0	1	(C5h)	VCOM control 1 nVM: VCOM input select VMH: VCOMH voltage control
	1	↑	1	-	nVM	VMH6	VMH 5	VMH4	VMH3	VMH2	VMH1	VMH0		
VMCTR2	0	↑	1	-	1	0	1	1	0	1	1	0	(C6h)	VCOM control 2 VMA: VCOMAC voltage control
	1	↑	1	-	0	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0		
	1	↑	1	-	nVM	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0		
RVMOF CTR	0	**1**	↑	-	1	0	1	1	1	0	0	0	(C8h)	VCOM control 4 Read the VMOF value form NV memory
	1	**1**	↑	-	nVM	RVMF 6	RVMF 5	RVMF 4	RVMF 3	RVMF 2	RVMF 1	RVMF 0		

"-": Don't care, can be set to VDDI or DGND level

Table 6.1.2 Panel Function Command List (3)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	Panel version code Write ID2 value to NV memory Set the LCM version code at ID2
	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
WRID3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Driver maker Project code Write ID3 value to NV memory Set the project code at ID3
	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
RDID4	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)	IC Vender Coder Dummy read ID41:IC Vender Coder ID42: IC Part Number Coder ID43 & ID44: Chip version coder
	1	1	↑	-	-	-	-	-	-	-	-	-		
	1	1	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410		
	1	1	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420		
	1	1	↑	-	ID437	ID436	ID435	ID434	ID43	ID432	ID431	ID430		
	1	1	↑	-	ID447	ID446	ID445	ID444	ID443	ID442	ID441	ID440		
NVCTR1	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)	NV memory function controller 1 Please refer to 'OTP programming procedure' for details.
				-										
NVCTR2	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	NV memory function controller 2 Please refer to 'OTP programming procedure' for details.
	1	↑	1	-										
NVCTR3	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	NV memory function controller 3 Please refer to 'OTP programming procedure' for details.
	1	↑	1	-										

"-": Don't care, can be set to VDDI or DGND level

Table 6.1.2 Panel Function Command List (4)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	R+ Gamma adjustment
	1	↑	1	-	-	-	-	R_PVR1V0[4]	R_PVR1V0[3]	R_PVR1V0[2]	R_PVR1V0[1]	R_PVR1V0[0]		
	1	↑	1	-	-	-	R_PVR1V1[5]	R_PVR1V1[4]	R_PVR1V1[3]	R_PVR1V1[2]	R_PVR1V1[1]	R_PVR1V1[0]		
	1	↑	1	-	-	-	R_PVR1V2[5]	R_PVR1V2[4]	R_PVR1V2[3]	R_PVR1V2[2]	R_PVR1V2[1]	R_PVR1V2[0]		
	1	↑	1	-	-	-	R_PVR1V61[5]	R_PVR1V61[4]	R_PVR1V61[3]	R_PVR1V61[2]	R_PVR1V61[1]	R_PVR1V61[0]		
	1	↑	1	-	-	-	R_PVR1V62[5]	R_PVR1V62[4]	R_PVR1V62[3]	R_PVR1V62[2]	R_PVR1V62[1]	R_PVR1V62[0]		
	1	↑	1	-	-	-	-	R_PVR1V63[4]	R_PVR1V63[3]	R_PVR1V63[2]	R_PVR1V63[1]	R_PVR1V63[0]		
	1	↑	1	-	-	-	-	R_PVR2V13[4]	R_PVR2V13[3]	R_PVR2V13[2]	R_PVR2V13[1]	R_PVR2V13[0]		
	1	↑	1	-	-	-	-	R_PVR2V50[4]	R_PVR2V50[3]	R_PVR2V50[2]	R_PVR2V50[1]	R_PVR2V50[0]		
	1	↑	1	-	-	-	-	-	R_PVR3V4[3]	R_PVR3V4[2]	R_PVR3V4[1]	R_PVR3V4[0]		
	1	↑	1	-	-	-	-	-	R_PVR3V8[3]	R_PVR3V8[2]	R_PVR3V8[1]	R_PVR3V8[0]		
	1	↑	1	-	-	-	-	-	R_PVR3V20[3]	R_PVR3V20[2]	R_PVR3V20[1]	R_PVR3V20[0]		
	1	↑	1	-	-	-	-	-	R_PVR3V27[3]	R_PVR3V27[2]	R_PVR3V27[1]	R_PVR3V27[0]		
	1	↑	1	-	-	-	-	-	R_PVR3V36[3]	R_PVR3V36[2]	R_PVR3V36[1]	R_PVR3V36[0]		
	1	↑	1	-	-	-	-	-	R_PVR3V43[3]	R_PVR3V43[2]	R_PVR3V43[1]	R_PVR3V43[0]		
	1	↑	1	-	-	-	-	-	R_PVR3V55[3]	R_PVR3V55[2]	R_PVR3V55[1]	R_PVR3V55[0]		
	1	↑	1	-	-	-	-	-	R_PVR3V59[3]	R_PVR3V59[2]	R_PVR3V59[1]	R_PVR3V59[0]		

"-": Don't care, can be set to VDDI or DGND level

Table 6.1.2 Panel Function Command List (5)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRN1	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	R- Gamma adjustment
	1	↑	1	-	-	-	-	R_NVR1V0[4]	R_NVR1V0[3]	R_NVR1V0[2]	R_NVR1V0[1]	R_NVR1V0[0]		
	1	↑	1	-	-	-	R_NVR1V1[5]	R_NVR1V1[4]	R_NVR1V1[3]	R_NVR1V1[2]	R_NVR1V1[1]	R_NVR1V1[0]		
	1	↑	1	-	-	-	R_NVR1V2[5]	R_NVR1V2[4]	R_NVR1V2[3]	R_NVR1V2[2]	R_NVR1V2[1]	R_NVR1V2[0]		
	1	↑	1	-	-	-	R_NVR1V61[5]	R_NVR1V61[4]	R_NVR1V61[3]	R_NVR1V61[2]	R_NVR1V61[1]	R_NVR1V61[0]		
	1	↑	1	-	-	-	R_NVR1V62[5]	R_NVR1V62[4]	R_NVR1V62[3]	R_NVR1V62[2]	R_NVR1V62[1]	R_NVR1V62[0]		
	1	↑	1	-	-	-	-	R_NVR1V63[4]	R_NVR1V63[3]	R_NVR1V63[2]	R_NVR1V63[1]	R_NVR1V63[0]		
	1	↑	1	-	-	-	-	R_NVR2V13[4]	R_NVR2V13[3]	R_NVR2V13[2]	R_NVR2V13[1]	R_NVR2V13[0]		
	1	↑	1	-	-	-	-	R_NVR2V50[4]	R_NVR2V50[3]	R_NVR2V50[2]	R_NVR2V50[1]	R_NVR2V50[0]		
	1	↑	1	-	-	-	-	-	R_NVR3V4[3]	R_NVR3V4[2]	R_NVR3V4[1]	R_NVR3V4[0]		
	1	↑	1	-	-	-	-	-	R_NVR3V8[3]	R_NVR3V8[2]	R_NVR3V8[1]	R_NVR3V8[0]		
	1	↑	1	-	-	-	-	-	R_NVR3V20[3]	R_NVR3V20[2]	R_NVR3V20[1]	R_NVR3V20[0]		
	1	↑	1	-	-	-	-	-	R_NVR3V27[3]	R_NVR3V27[2]	R_NVR3V27[1]	R_NVR3V27[0]		
	1	↑	1	-	-	-	-	-	R_NVR3V36[3]	R_NVR3V36[2]	R_NVR3V36[1]	R_NVR3V36[0]		
	1	↑	1	-	-	-	-	-	R_NVR3V43[3]	R_NVR3V43[2]	R_NVR3V43[1]	R_NVR3V43[0]		
	1	↑	1	-	-	-	-	-	R_NVR3V55[3]	R_NVR3V55[2]	R_NVR3V55[1]	R_NVR3V55[0]		
	1	↑	1	-	-	-	-	-	R_NVR3V59[3]	R_NVR3V59[2]	R_NVR3V59[1]	R_NVR3V59[0]		

"-": Don't care, can be set to VDDI or DGND level

Table 6.1.2 Panel Function Command List (6)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E2h)	G+ Gamma adjustment
	1	↑	1	-	-	-	-	G_PVR1V0[4]	G_PVR1V0[3]	G_PVR1V0[2]	G_PVR1V0[1]	G_PVR1V0[0]		
	1	↑	1	-	-	-	G_PVR1V1[5]	G_PVR1V1[4]	G_PVR1V1[3]	G_PVR1V1[2]	G_PVR1V1[1]	G_PVR1V1[0]		
	1	↑	1	-	-	-	G_PVR1V2[5]	G_PVR1V2[4]	G_PVR1V2[3]	G_PVR1V2[2]	G_PVR1V2[1]	G_PVR1V2[0]		
	1	↑	1	-	-	-	G_PVR1V61[5]	G_PVR1V61[4]	G_PVR1V61[3]	G_PVR1V61[2]	G_PVR1V61[1]	G_PVR1V61[0]		
	1	↑	1	-	-	-	G_PVR1V62[5]	G_PVR1V62[4]	G_PVR1V62[3]	G_PVR1V62[2]	G_PVR1V62[1]	G_PVR1V62[0]		
	1	↑	1	-	-	-	-	G_PVR1V63[4]	G_PVR1V63[3]	G_PVR1V63[2]	G_PVR1V63[1]	G_PVR1V63[0]		
	1	↑	1	-	-	-	-	G_PVR2V13[4]	G_PVR2V13[3]	G_PVR2V13[2]	G_PVR2V13[1]	G_PVR2V13[0]		
	1	↑	1	-	-	-	-	G_PVR2V50[4]	G_PVR2V50[3]	G_PVR2V50[2]	G_PVR2V50[1]	G_PVR2V50[0]		
	1	↑	1	-	-	-	-	-	G_PVR3V4[3]	G_PVR3V4[2]	G_PVR3V4[1]	G_PVR3V4[0]		
	1	↑	1	-	-	-	-	-	G_PVR3V8[3]	G_PVR3V8[2]	G_PVR3V8[1]	G_PVR3V8[0]		
	1	↑	1	-	-	-	-	-	G_PVR3V20[3]	G_PVR3V20[2]	G_PVR3V20[1]	G_PVR3V20[0]		
	1	↑	1	-	-	-	-	-	G_PVR3V27[3]	G_PVR3V27[2]	G_PVR3V27[1]	G_PVR3V27[0]		
	1	↑	1	-	-	-	-	-	G_PVR3V36[3]	G_PVR3V36[2]	G_PVR3V36[1]	G_PVR3V36[0]		
	1	↑	1	-	-	-	-	-	G_PVR3V43[3]	G_PVR3V43[2]	G_PVR3V43[1]	G_PVR3V43[0]		
	1	↑	1	-	-	-	-	-	G_PVR3V55[3]	G_PVR3V55[2]	G_PVR3V55[1]	G_PVR3V55[0]		
	1	↑	1	-	-	-	-	-	G_PVR3V59[3]	G_PVR3V59[2]	G_PVR3V59[1]	G_PVR3V59[0]		

“-“: Don’t care, can be set to VDDI or DGND level

Table 6.1.2 Panel Function Command List (7)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRN1	0	↑	1	-	1	1	1	0	0	0	0	1	(E3h)	G- Gamma adjustment
	1	↑	1	-	-	-	-	G_NVR1V0[4]	G_NVR1V0[3]	G_NVR1V0[2]	G_NVR1V0[1]	G_NVR1V0[0]		
	1	↑	1	-	-	-	G_NVR1V1[5]	G_NVR1V1[4]	G_NVR1V1[3]	G_NVR1V1[2]	G_NVR1V1[1]	G_NVR1V1[0]		
	1	↑	1	-	-	-	G_NVR1V2[5]	G_NVR1V2[4]	G_NVR1V2[3]	G_NVR1V2[2]	G_NVR1V2[1]	G_NVR1V2[0]		
	1	↑	1	-	-	-	G_NVR1V61[5]	G_NVR1V61[4]	G_NVR1V61[3]	G_NVR1V61[2]	G_NVR1V61[1]	G_NVR1V61[0]		
	1	↑	1	-	-	-	G_NVR1V62[5]	G_NVR1V62[4]	G_NVR1V62[3]	G_NVR1V62[2]	G_NVR1V62[1]	G_NVR1V62[0]		
	1	↑	1	-	-	-	-	G_NVR1V63[4]	G_NVR1V63[3]	G_NVR1V63[2]	G_NVR1V63[1]	G_NVR1V63[0]		
	1	↑	1	-	-	-	-	G_NVR2V13[4]	G_NVR2V13[3]	G_NVR2V13[2]	G_NVR2V13[1]	G_NVR2V13[0]		
	1	↑	1	-	-	-	-	G_NVR2V50[4]	G_NVR2V50[3]	G_NVR2V50[2]	G_NVR2V50[1]	G_NVR2V50[0]		
	1	↑	1	-	-	-	-	-	G_NVR3V4[3]	G_NVR3V4[2]	G_NVR3V4[1]	G_NVR3V4[0]		
	1	↑	1	-	-	-	-	-	G_NVR3V8[3]	G_NVR3V8[2]	G_NVR3V8[1]	G_NVR3V8[0]		
	1	↑	1	-	-	-	-	-	G_NVR3V20[3]	G_NVR3V20[2]	G_NVR3V20[1]	G_NVR3V20[0]		
	1	↑	1	-	-	-	-	-	G_NVR3V27[3]	G_NVR3V27[2]	G_NVR3V27[1]	G_NVR3V27[0]		
	1	↑	1	-	-	-	-	-	G_NVR3V36[3]	G_NVR3V36[2]	G_NVR3V36[1]	G_NVR3V36[0]		
	1	↑	1	-	-	-	-	-	G_NVR3V43[3]	G_NVR3V43[2]	G_NVR3V43[1]	G_NVR3V43[0]		
	1	↑	1	-	-	-	-	-	G_NVR3V55[3]	G_NVR3V55[2]	G_NVR3V55[1]	G_NVR3V55[0]		
	1	↑	1	-	-	-	-	-	G_NVR3V59[3]	G_NVR3V59[2]	G_NVR3V59[1]	G_NVR3V59[0]		

“-“: Don’t care, can be set to VDDI or DGND level

Table 6.1.2 Panel Function Command List (8)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E4h)	B+ Gamma adjustment
	1	↑	1	-	-	-	-	B_PVR1V0[4]	B_PVR1V0[3]	B_PVR1V0[2]	B_PVR1V0[1]	B_PVR1V0[0]		
	1	↑	1	-	-	-	B_PVR1V1[5]	B_PVR1V1[4]	B_PVR1V1[3]	B_PVR1V1[2]	B_PVR1V1[1]	B_PVR1V1[0]		
	1	↑	1	-	-	-	B_PVR1V2[5]	B_PVR1V2[4]	B_PVR1V2[3]	B_PVR1V2[2]	B_PVR1V2[1]	B_PVR1V2[0]		
	1	↑	1	-	-	-	B_PVR1V61[5]	B_PVR1V61[4]	B_PVR1V61[3]	B_PVR1V61[2]	B_PVR1V61[1]	B_PVR1V61[0]		
	1	↑	1	-	-	-	B_PVR1V62[5]	B_PVR1V62[4]	B_PVR1V62[3]	B_PVR1V62[2]	B_PVR1V62[1]	B_PVR1V62[0]		
	1	↑	1	-	-	-	-	B_PVR1V63[4]	B_PVR1V63[3]	B_PVR1V63[2]	B_PVR1V63[1]	B_PVR1V63[0]		
	1	↑	1	-	-	-	-	B_PVR2V13[4]	B_PVR2V13[3]	B_PVR2V13[2]	B_PVR2V13[1]	B_PVR2V13[0]		
	1	↑	1	-	-	-	-	B_PVR2V50[4]	B_PVR2V50[3]	B_PVR2V50[2]	B_PVR2V50[1]	B_PVR2V50[0]		
	1	↑	1	-	-	-	-	-	B_PVR3V4[3]	B_PVR3V4[2]	B_PVR3V4[1]	B_PVR3V4[0]		
	1	↑	1	-	-	-	-	-	B_PVR3V8[3]	B_PVR3V8[2]	B_PVR3V8[1]	B_PVR3V8[0]		
	1	↑	1	-	-	-	-	-	B_PVR3V20[3]	B_PVR3V20[2]	B_PVR3V20[1]	B_PVR3V20[0]		
	1	↑	1	-	-	-	-	-	B_PVR3V27[3]	B_PVR3V27[2]	B_PVR3V27[1]	B_PVR3V27[0]		
	1	↑	1	-	-	-	-	-	B_PVR3V36[3]	B_PVR3V36[2]	B_PVR3V36[1]	B_PVR3V36[0]		
	1	↑	1	-	-	-	-	-	B_PVR3V43[3]	B_PVR3V43[2]	B_PVR3V43[1]	B_PVR3V43[0]		
	1	↑	1	-	-	-	-	-	B_PVR3V55[3]	B_PVR3V55[2]	B_PVR3V55[1]	B_PVR3V55[0]		
	1	↑	1	-	-	-	-	-	B_PVR3V59[3]	B_PVR3V59[2]	B_PVR3V59[1]	B_PVR3V59[0]		

"-": Don't care, can be set to VDDI or DGND level

Table 6.1.2 Panel Function Command List (9)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRN1	0	↑	1	-	1	1	1	0	0	0	0	1	(E5h)	B- Gamma adjustment
	1	↑	1	-	-	-	-	B_NVR1V0[4]	B_NVR1V0[3]	B_NVR1V0[2]	B_NVR1V0[1]	B_NVR1V0[0]		
	1	↑	1	-	-	-	B_NVR1V1[5]	B_NVR1V1[4]	B_NVR1V1[3]	B_NVR1V1[2]	B_NVR1V1[1]	B_NVR1V1[0]		
	1	↑	1	-	-	-	B_NVR1V2[5]	B_NVR1V2[4]	B_NVR1V2[3]	B_NVR1V2[2]	B_NVR1V2[1]	B_NVR1V2[0]		
	1	↑	1	-	-	-	B_NVR1V61[5]	B_NVR1V61[4]	B_NVR1V61[3]	B_NVR1V61[2]	B_NVR1V61[1]	B_NVR1V61[0]		
	1	↑	1	-	-	-	B_NVR1V62[5]	B_NVR1V62[4]	B_NVR1V62[3]	B_NVR1V62[2]	B_NVR1V62[1]	B_NVR1V62[0]		
	1	↑	1	-	-	-	-	B_NVR1V63[4]	B_NVR1V63[3]	B_NVR1V63[2]	B_NVR1V63[1]	B_NVR1V63[0]		
	1	↑	1	-	-	-	-	B_NVR2V13[4]	B_NVR2V13[3]	B_NVR2V13[2]	B_NVR2V13[1]	B_NVR2V13[0]		
	1	↑	1	-	-	-	-	B_NVR2V50[4]	B_NVR2V50[3]	B_NVR2V50[2]	B_NVR2V50[1]	B_NVR2V50[0]		
	1	↑	1	-	-	-	-	-	B_NVR3V4[3]	B_NVR3V4[2]	B_NVR3V4[1]	B_NVR3V4[0]		
	1	↑	1	-	-	-	-	-	B_NVR3V8[3]	B_NVR3V8[2]	B_NVR3V8[1]	B_NVR3V8[0]		
	1	↑	1	-	-	-	-	-	B_NVR3V20[3]	B_NVR3V20[2]	B_NVR3V20[1]	B_NVR3V20[0]		
	1	↑	1	-	-	-	-	-	B_NVR3V27[3]	B_NVR3V27[2]	B_NVR3V27[1]	B_NVR3V27[0]		
	1	↑	1	-	-	-	-	-	B_NVR3V36[3]	B_NVR3V36[2]	B_NVR3V36[1]	B_NVR3V36[0]		
	1	↑	1	-	-	-	-	-	B_NVR3V43[3]	B_NVR3V43[2]	B_NVR3V43[1]	B_NVR3V43[0]		
	1	↑	1	-	-	-	-	-	B_NVR3V55[3]	B_NVR3V55[2]	B_NVR3V55[1]	B_NVR3V55[0]		
	1	↑	1	-	-	-	-	-	B_NVR3V59[3]	B_NVR3V59[2]	B_NVR3V59[1]	B_NVR3V59[0]		

"-": Don't care, can be set to VDDI or DGND level

6.2. System Command Description

6.2.1. NOP (00h)

00H	**NOP (No Operation)**												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00H)
Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is empty command. It does not have effect on the display module. -However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMHD (Memory Read) and parameter write commands.
Restriction	-
Register Availability	see table below
Default	see table below
Flow Chart	-

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

6.2.2. SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01H)
Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description) *Note: The Frame Memory contents are not affected by this command.*
Restriction	-It will be necessary to wait 5msec before sending new command following software reset. -The display module loads all display supplier's factory default values to the registers during 5msec. -If Software Reset is applied during Sleep Out mode, it will be necessary to wait *120msec* before sending Sleep Out command. -Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	see table below
Default	see table below
Flow Chart	see figure below

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart:

6.2.3. RDDID (04H): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04H)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h
3rd Parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h
4th Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	62h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This read byte returns 18-bits display identification information.

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

-The 3rd parameter (ID27 to ID20): LCD module/driver version ID

-The 4th parameter (ID37 to UD30): LCD module/driver ID.

NOTE: Commands RDID1/2/3 (DAH, DBH, DCH) read data correspond to the parameters 2,3,4 of the command 04H, respectively.

Restriction

-

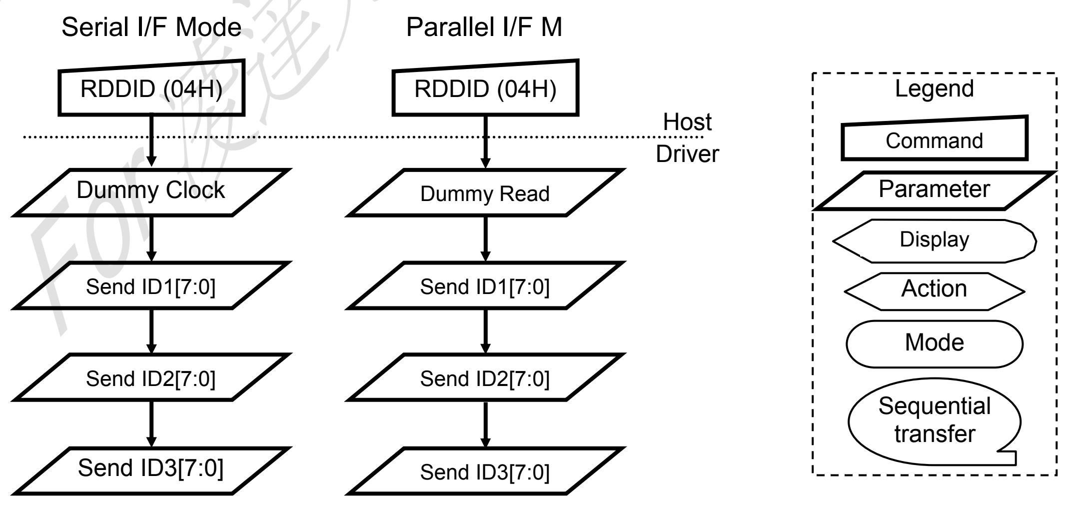
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	38h	38h	38h
S/W Reset	80h	80h	80h
H/W Reset	62h	62h	62h

Flow Chart



6.2.4. RDDST (09H): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09H)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	ST25	ST24	00h
3rd Parameter	1	1	↑	-	ST23	PF2	PF1	PF0	IDMON	PTLON	SLOUT	NORON	61h
4th Parameter	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	00h
5th Parameter	1	1	↑		GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36H) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36H) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36H) D6='1') '0' =Increment, (Left to Right, when MADCTL (36H) D6='0')
MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36H) D5='1') '0' = Normal, (when MADCTL (36H) D5='0')
ML	Vertical Refresh Order (ML)	'1' =Decrement, (LCD refresh Bottom to Top, when MADCTL (36H) D4='1') "0"=Increment, (LCD refresh Top to Bottom, when MADCTL (36H) D4='0')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36H) D3='1') '0' =RGB, (When MADCTL (36H) D3='0')
ST25	For Future Use	'0'
ST24	For Future Use	'0'
ST23	For Future Use	'0'
PF2 PF1 PF0	Color Pixel Format Definition	"011" = 12-bits / pixel, "101" = 16-bits / pixel, "110" = 18-bits / pixel, others are no define
IDMON	Idle Mode On/Off	'1' = On, "0" = Off
PTLON	Partial Mode On/Off	'1' = On, "0" = Off
SLPOUT	Sleep In/Out	'1' = Out, "0" = In
NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
VSSON	Vertical Scrolling Status	'1' = Scroll on,"0" = Scroll off
ST14	For Future Use	'0'
INVON	Inversion Status	'1' = On, "0" = Off
ST12	For Future Use	'0'
ST11	For Future Use	'0'
DISON	Display On/Off	'1' = On, "0" = Off
TEON	Tearing effect line on/off	'1' = On, "0" = Off
GCSEL2 GCSEL1 GCSEL0	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3, "100" to "111" = Not defined
TELOM	Tearing effect line mode	'0' = mode1, '1' = mode2
HSON	Horizontal Sync. (HS)	'1' = On, '0' = Off
VSON	Vertical Sync, (VS, RGB I/F)	'1' = On, '0' = Off
PCLKON	Pixel Clock (PCLK, RGB I/F)	'1' = On, '0' = Off
DEON	Data Enable (DE, RGB I/F)	'1' = On, '0' = Off
ST0	For Future Use	'0'

Note: ST0, ST11-ST12, ST14, ST23, ST24 are set to '0'

Restriction	-

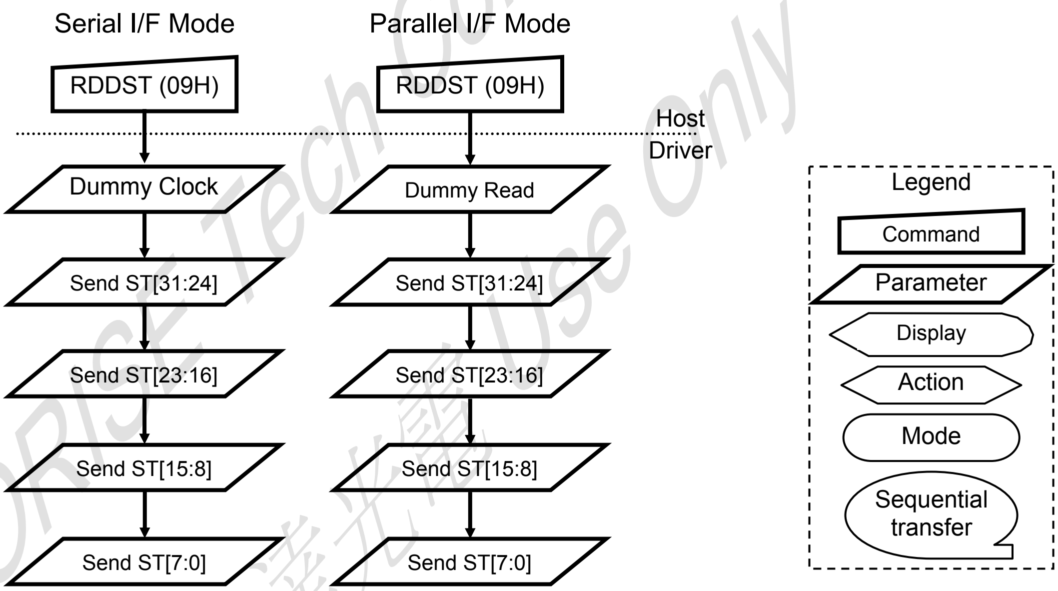
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0)			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx-xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

Flow Chart



6.2.5. RDDPM (0AH): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0AH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	08h-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	"1"=Booster on, "0"=Booster off
IDMON	Idle Mode On/Off	"1" = Idle Mode On, "0" = Idle Mode Off
PTLON	Partial Mode On/Off	"1" = Partial Mode On, "0" = Partial Mode Off
SLPON	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In
NORON	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
DISON	Display On/Off	"1" = Display On, "0" = Display Off
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

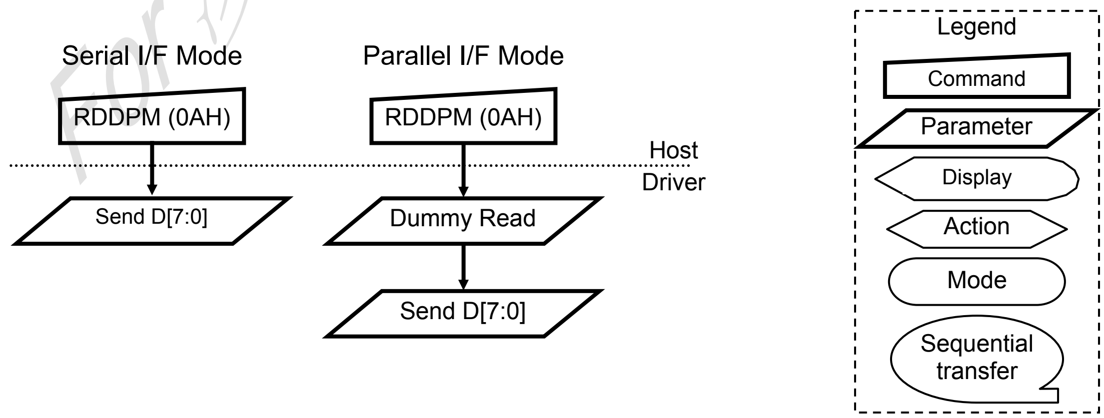
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000 (08h)
S/W Reset	0000_1000 (08h)
H/W Reset	0000_1000 (08h)

Flow Chart



6.2.6. RDDMADCTR (0BH): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTR	0	↑	1	-	0	0	0	0	1	0	1	1	(0BH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑		MX	MY	MV	ML	RGB	D2	D1	D0	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
MX	Row Address Order	'1' =Decrement, "0"=Increment
MY	Column Address Order	'1' =Decrement, "0"=Increment
MV	Row/Column Order (MV)	'1' = Row/column exchange (MV=1) '0' = Normal (MV=0)
ML	Vertical Refresh Order	'1' =LCD Refresh Top to Bottom '0' =LCD Refresh Bottom to Top
RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

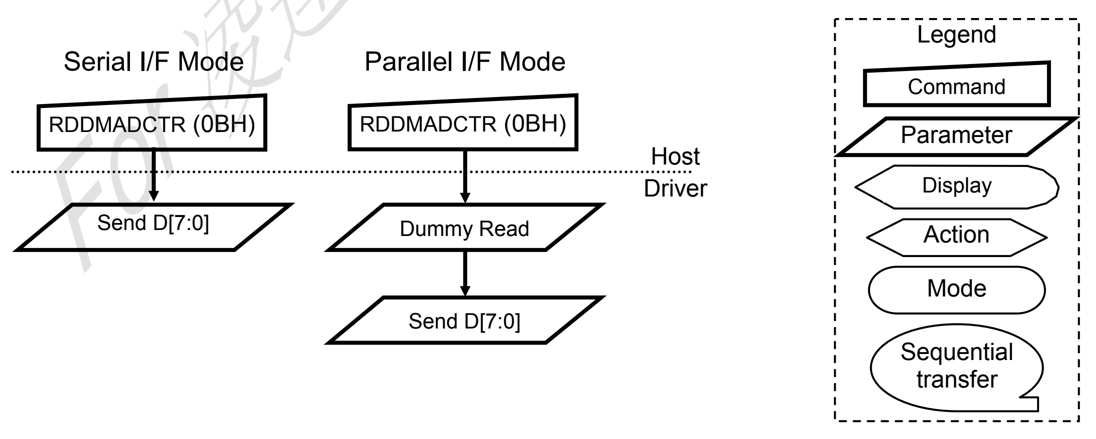
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change
H/W Reset	0000_0000 (00h)

Flow Chart



6.2.7. RDDCOLMOD (0CH): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0CH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command indicates the current status of the display as described in the table below:

IFPF[2:0]		MCU Interface Color Format
011	3	12-bits/pixel
101	5	16-bits/pixel
110	6	18-bits/pixel
111	7	Reserved

Others are no define and invalid

VIPF[3:0]		RGB Interface Color Format
0101	5	16-bits/pixel (1-times data transfer)
0110	6	18-bits/pixel (1-times data transfer)
0111	7	Reserved
1110	14	18-bits/pixel (3-times data transfer)

Others are no define and invalid

Restriction

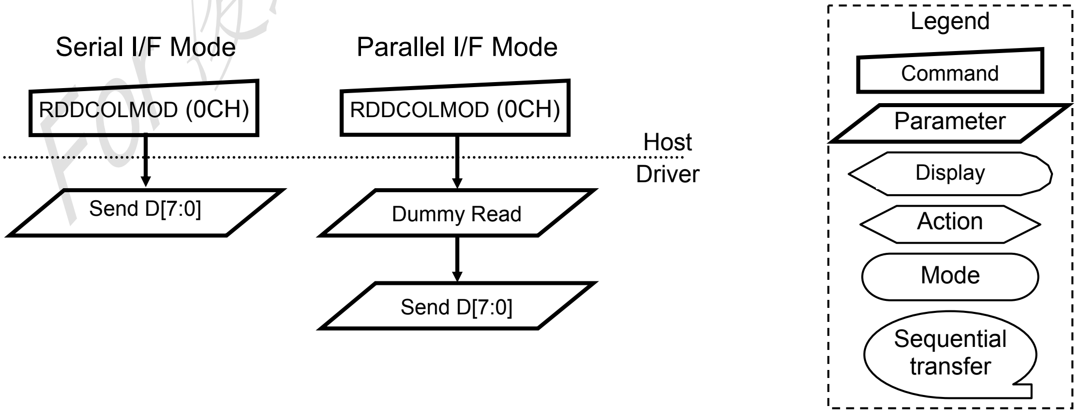
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	IFPF[2:0]	VIPF[3:0]
Power On Sequence	0101 (16-bits/pixel)	0110 (18-bits/pixel)
S/W Reset	No Change	No Change
H/W Reset	0101 (16-bits/pixel)	0110 (18-bits/pixel)

Flow Chart



6.2.8. RDDIM (0DH): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0DH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
VSSON	Vertical Scrolling On/Off	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	For Future Use	"0" (Not used)
INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	For Future Use	"0" (Not used)
D3	For Future Use	"0" (Not used)
GCS2 GCS1 GCS0	Gamma Curve Selection	"000" = GC0, "001" = GC1, "010" = GC2, "011" = GC3, "100" to "111" = Not defined

Restriction

-

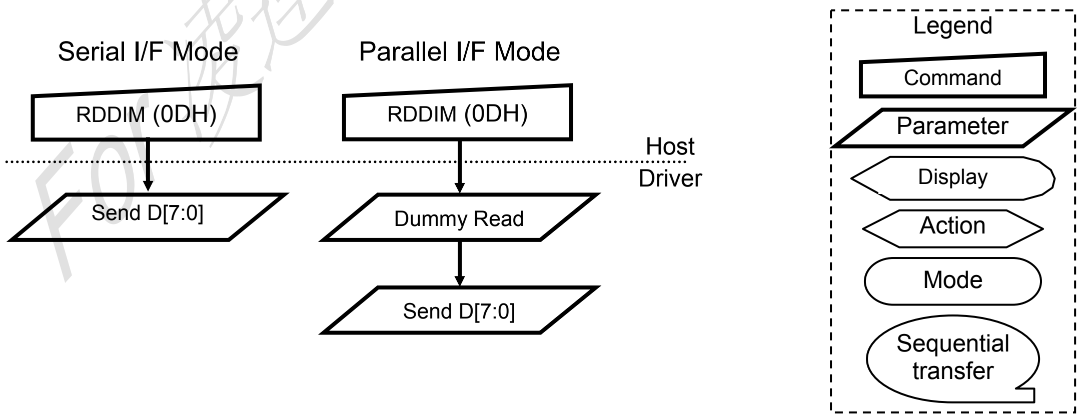
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



6.2.9. RDDSM (0EH): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0EH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing Effect Line On/Off	"1" = On, "0" = Off
TELOM	Tearing effect line mode	"0" = mode1, "1" = mode2
HSON	Horizontal Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
VSON	Vertical Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
PCKON	Pixel Clock (PCLK, RGB I/F) On/Off	"1" = On, "0" = Off
DEON	Data Enable (DE, RGB I/F) On/Off	"1" = On, "0" = Off
D1	Not Used	"1" = On, "0" = Off
D0	Not Used	"1" = On, "0" = Off

Restriction

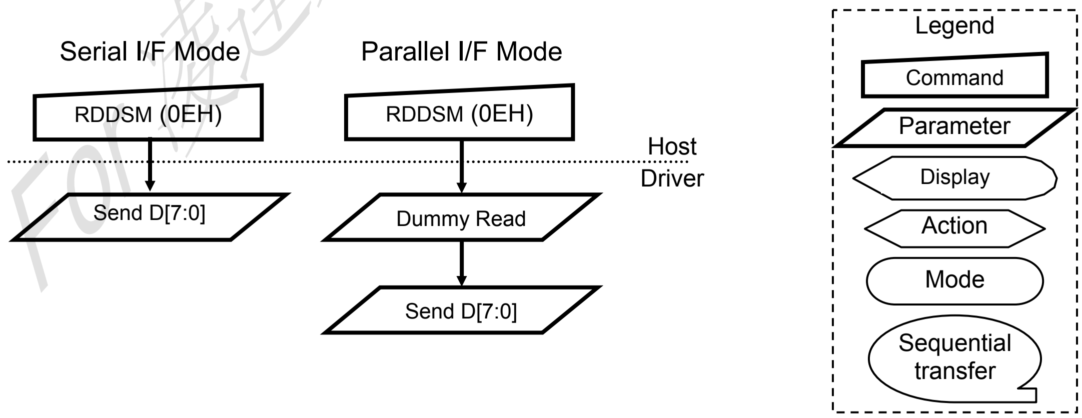
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



6.2.10. RDDSDR (0FH): Read Display Self-Diagnostic Result

0FH	RDDSDR (Read Display Self-Diagnostic Result)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0FH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
RELD	Register Loading Detection	See section 6.15.1
FUND	Functionality Detection	See section 6.15.1
ATTD	Chip Attachment Detection	See section 6.15.3
BRD	Display Glass Break Detection	See section 6.15.4
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

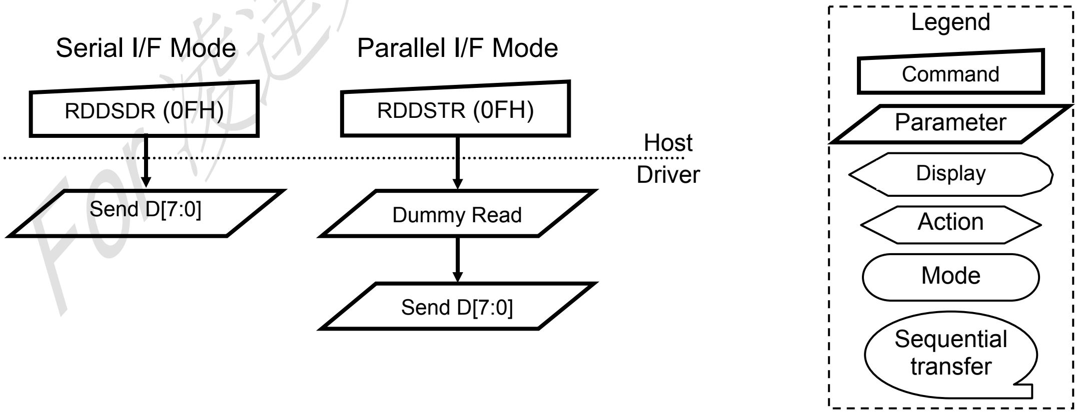
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

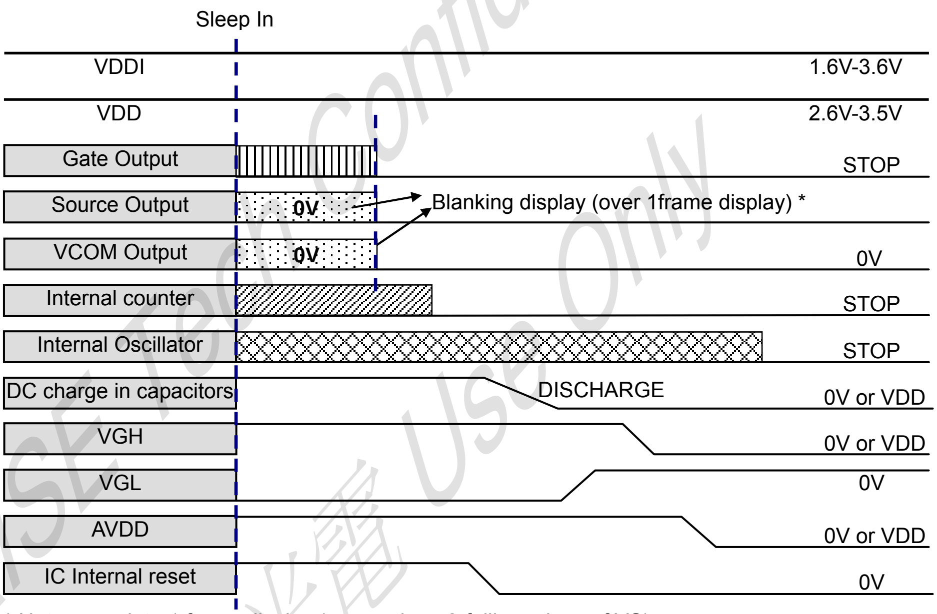
Flow Chart



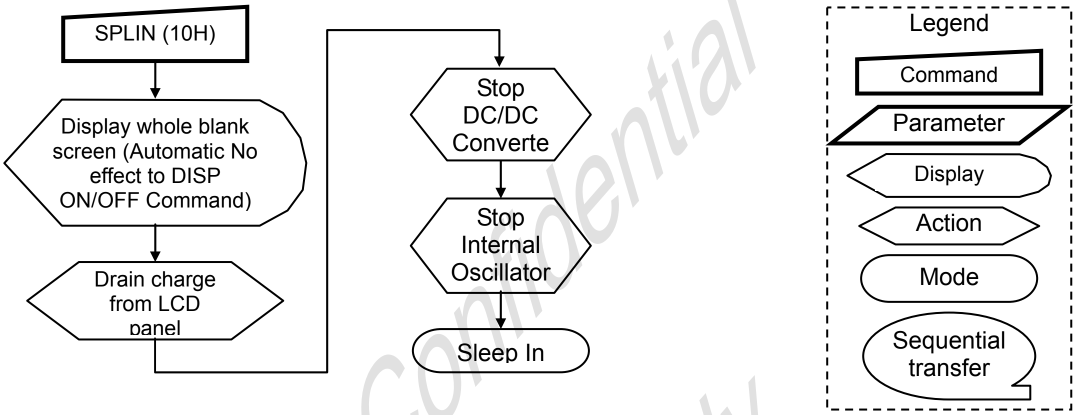
6.2.11. SLPIN (10H): Sleep In

10H	SLPIN (Sleep In)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10H)
1st Parameter	No parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

<table>
<tr><td>Description</td><td>
-This command causes the LCD module to enter the minimum power consumption mode.
-In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.


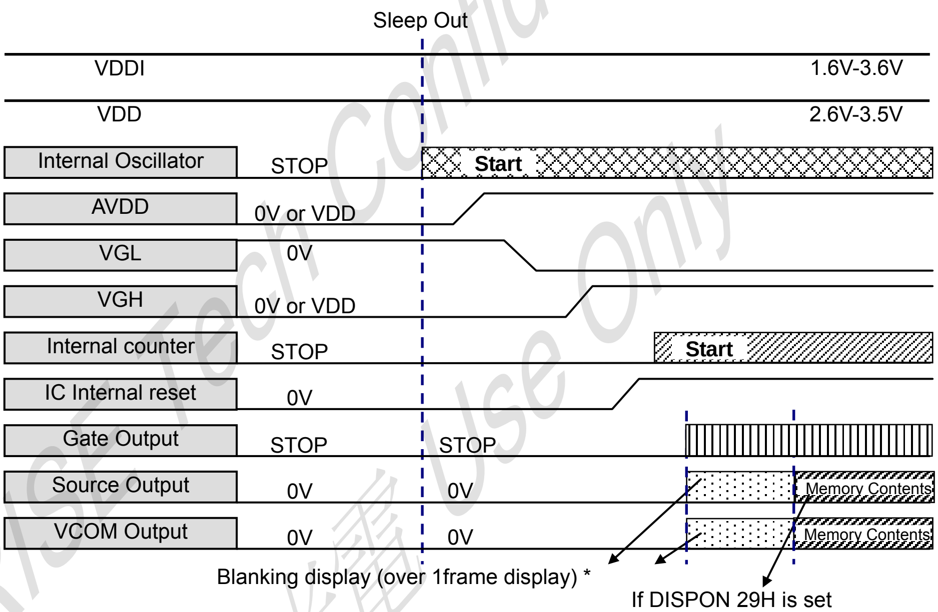
* Note: complete 1 frame display (ex: continue 2-falling edges of VS)
<u>-MCU interface and memory are still working and the memory keeps its contents</u>
</td></tr>
<tr><td>Restriction</td><td>
-This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11H).
-It will be necessary to wait <u>5msec</u> before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
-It will be necessary to wait <u>120msec</u> after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.
</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Sleep In mode</td></tr>
<tr><td>S/W Reset</td><td>Sleep In mode</td></tr>
<tr><td>H/W Reset</td><td>Sleep In mode</td></tr>
</table>
</td></tr>
</table>

Flow Chart	-It takes about 120msec to get into Sleep In mode (booster off state) after SLPIN command issued. -The results of booster off can be check by RDDST (09H) command Bit31. 

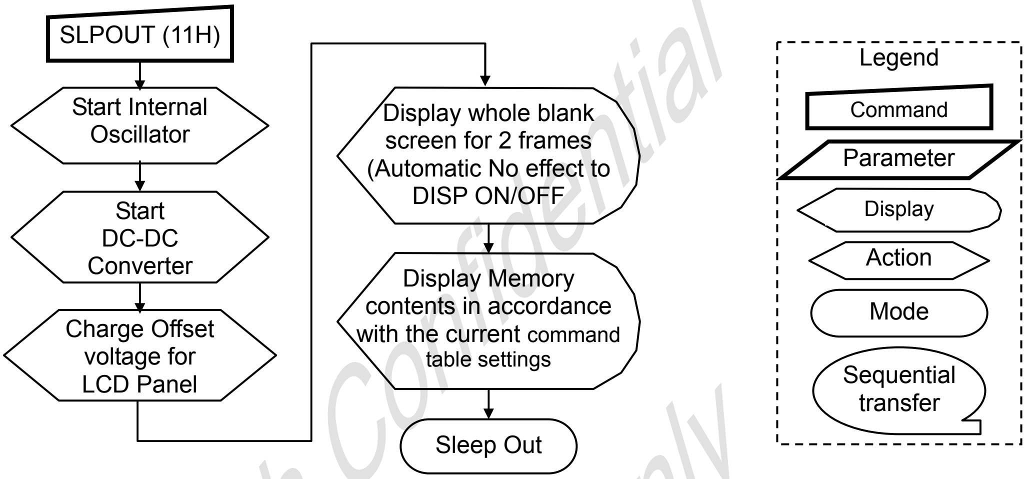
6.2.12. SLPOUT (11H): Sleep Out

11H	SLPOUT (Sleep Out)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

<table>
<tr><td>Description</td><td>-This command turns off sleep mode.
-In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.


* Note: complete 1 frame display (ex: continue 2-falling edges of VS)</td></tr>
<tr><td>Restriction</td><td>-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10H).
-It will be necessary to wait <u>5msec</u> before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
-DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode.
-DRIVER is doing self-diagnostic functions during this <u>5msec</u>. See also section 8.19.
-It will be necessary to wait <u>120msec</u> after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent</td></tr>
<tr><td>Register Availability</td><td><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In mode</td></tr><tr><td>S/W Reset</td><td>Sleep In mode</td></tr><tr><td>H/W Reset</td><td>Sleep In mode</td></tr></table></td></tr>
</table>

Flow Chart	-It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. -The results of booster on can be checked by RDDST (09H) command Bit31. 

6.2.13. PTLON (12H): Partial Display Mode On

12H	PTLON (Partial Display Mode On)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) -To leave Partial mode, the Normal Display Mode On command (13H) should be written. -There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availability	(see table below)
Default	(see table below)
Flow Chart	See Partial Area (30H)

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

6.2.14. NORON (13H): Normal Display Mode On

13H	NORON (Normal Display Mode On)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

<table>
<tr><td>Description</td><td>-This command returns the display to normal mode.
-Normal display mode on means Partial mode off, Scroll mode Off.
-Exit from NORON by the Partial mode On command (12H)
-There is no abnormal visual effect during mode change from Normal mode On to Partial mode On.</td></tr>
<tr><td>Restriction</td><td>-This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td>-See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command</td></tr>
</table>

6.2.15. INVOFF (20H): Display Inversion Off

20H	INVOFF (Display Inversion Off)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20H)
1st Parameter	No Parameter												-

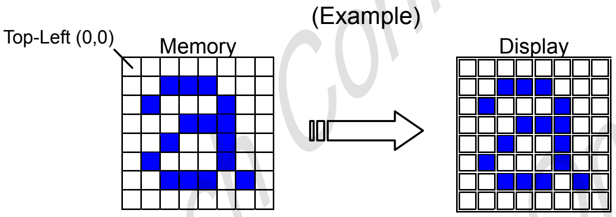
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to recover from display inversion mode.

-This command makes no change of contents of frame memory.

-This command does not change any other status.



Restriction

-This command has no effect when module is already inversion off mode.

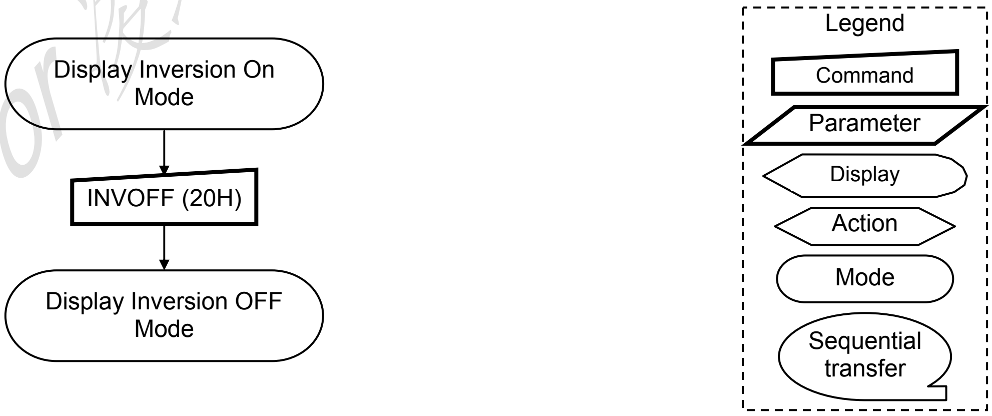
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



6.2.16. INVON (21H): Display Inversion On

21H	INVON (Display Inversion On)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

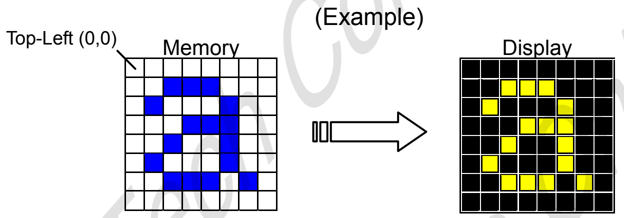
Description

-This command is used to enter into display inversion mode

-This command makes no change of contents of frame memory.

-This command does not change any other status.

-To exit from Display Inversion On, the Display Inversion Off command (20H) should be written.



Restriction

-This command has no effect when module is already Inversion On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart

6.2.17. GAMSET (26H): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26H)
1st Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in section 6.12. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC [7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (G2.2)
02h	GC1	Gamma Curve 2 (G1.8)
04h	GC2	Gamma Curve 3 (G2.5)
08h	GC3	Gamma Curve 4 (G1.0)

Note: All other values are undefined.

Restriction

-Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.

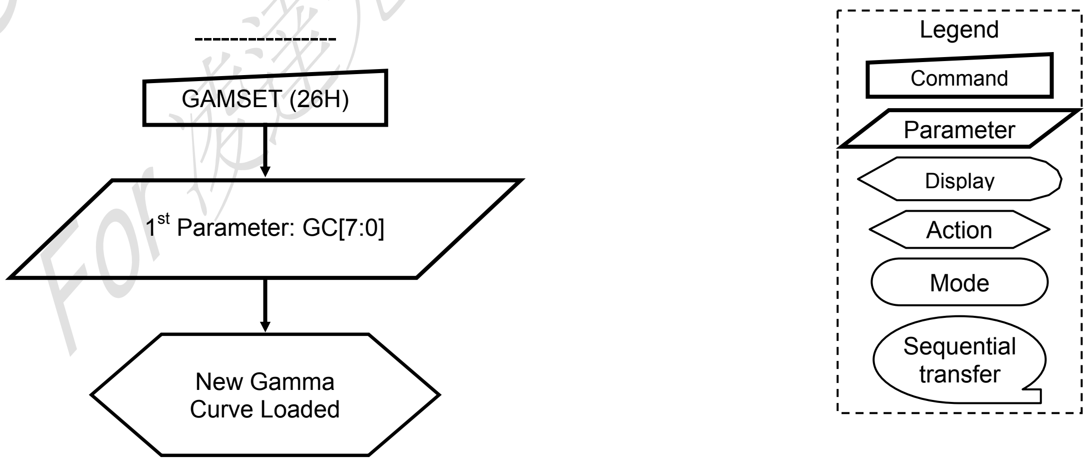
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



6.2.18. DISPOFF (28H): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.

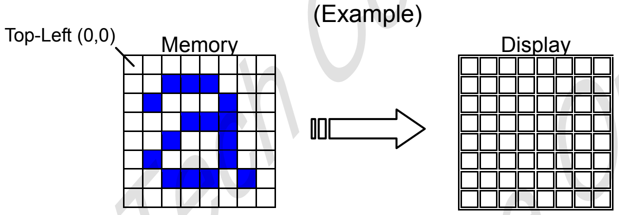
-This command makes no change of contents of frame memory.

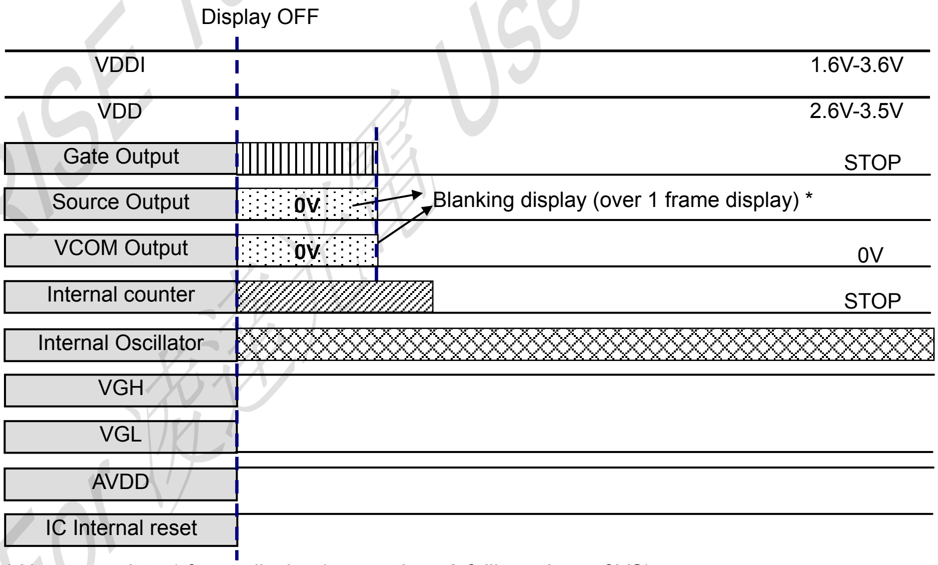
-This command does not change any other status.

-There will be no abnormal visible effect on the display.

-Exit from this command by Display On (29H)

(Example)





* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Restriction

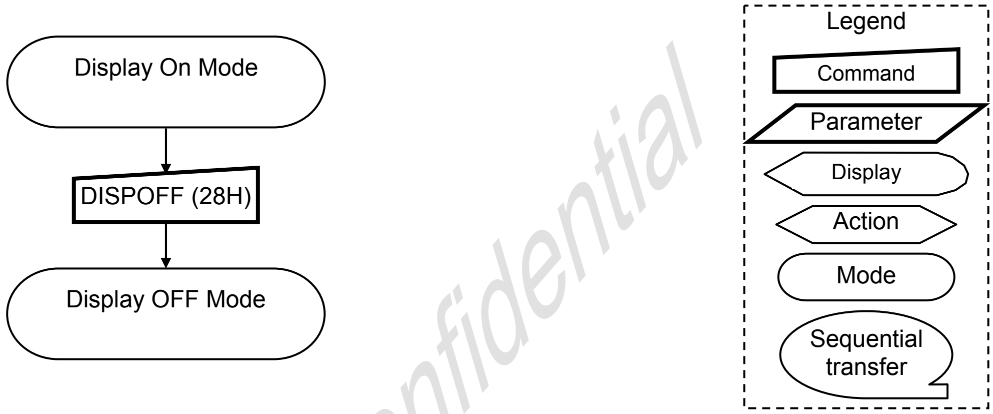
-This command has no effect when module is already in Display Off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	

Display On Mode
DISPOFF (28H)
Display OFF Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.19. DISPON (29H): Display On

29H	DISPON (Display On)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

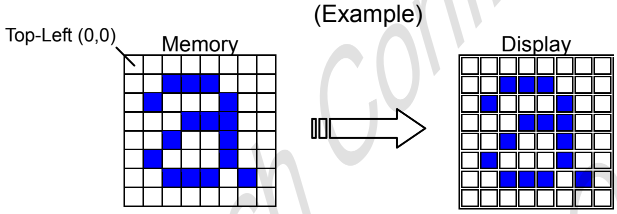
Description

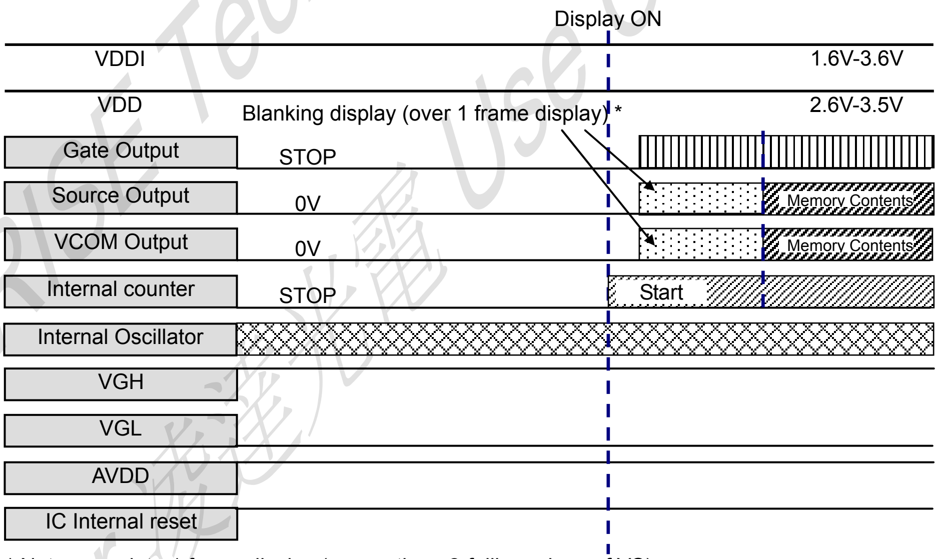
-This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.

-This command makes no change of contents of frame memory.

-This command does not change any other status.

(Example)





* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Restriction

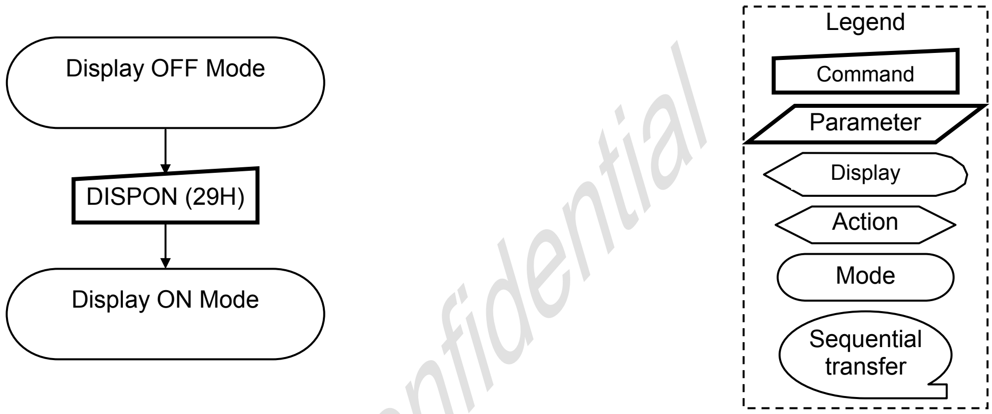
-This command has no effect when module is already in Display On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	Display OFF Mode DISPON (29H) Display ON Mode Legend Command Parameter Display Action Mode Sequential transfer

6.2.20. CASET (2AH): Column Address Set

2AH	CASET (Column Address Set)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2AH)
1st Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	00h
2nd Parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	00h
3rd Parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4th Parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

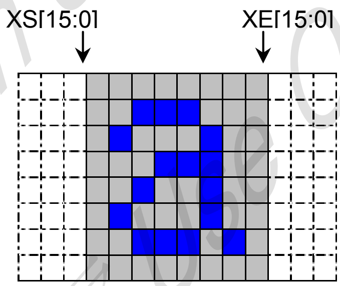
-This command is used to define area of frame memory where MCU can access.

-This command makes no change on the other driver status.

-The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.

-Each value represents one column line in the Frame Memory.

(Example)



Restriction

XS [15:0] always must be equal to or less than XE [15:0]

When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

1. 176x220 memory base (GM1, GM0 = "00")
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 175 (00AFh)): MV="0"
   If the "XS" or "XE" are large then 175d, it become 175d
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 219d (00DBh)): MV="1"
   If the "XS" or "XE" are large then 219d, it become 219d
2. 176x176 memory base (GM1, GM0 = "01")
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 175 (00AFh)): MV="0"
   If the "XS" or "XE" are large then 175d, it become 175d
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 175 (00AFh)): MV="1"
   If the "XS" or "XE" are large then 175d, it become 175d
1. 176x132 memory base (GM1, GM0 = "11")
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 175 (00AFh)): MV="0"
   If the "XS" or "XE" are large then 175d, it become 175d
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 131d (0083h)): MV="1"
   If the "XS" or "XE" are large then 131d, it become 131d

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176x220 memory base (GM1, GM0 = "00")

Status	Default Value		
	XS [15:0]	XE [15:0] (MV='**0**')	XE [15:0] (MV='**1**')
Power On Sequence	0000h	00AFh (175d)	
S/W Reset	0000h	00AFh (175d)	00DBh (219d)
H/W Reset	0000h	00AFh (175d)	

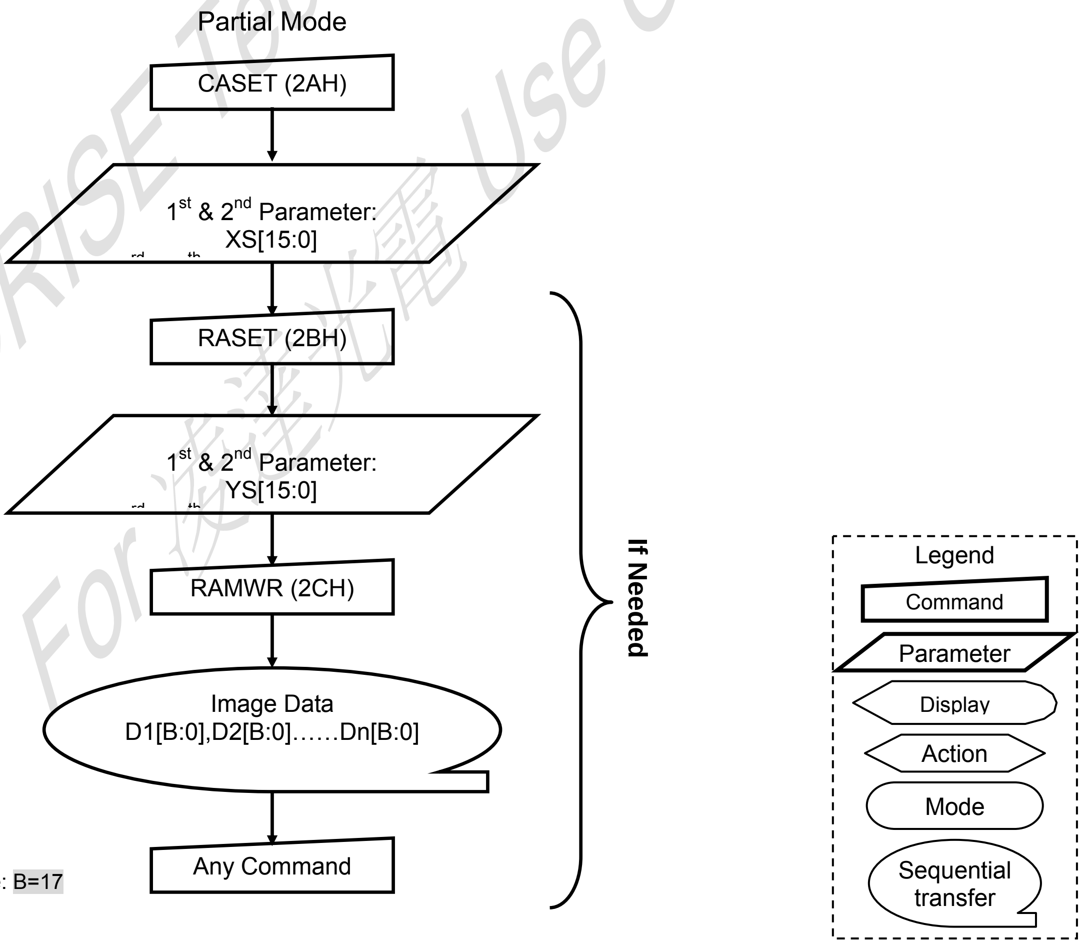
2. 176x176 memory base (GM1, GM0 = "01")

Status	Default Value		
	XS [15:0]	XE [15:0] (MV='**0**')	XE [15:0] (MV='**1**')
Power On Sequence	0000h	00AFh (175d)	
S/W Reset	0000h	00AFh (175d)	
H/W Reset	0000h	00AFh (175d)	

3. 176x132 memory base (GM1, GM0 = "11")

Status	Default Value		
	XS [15:0]	XE [15:0] (MV='**0**')	XE [15:0] (MV='**1**')
Power On Sequence	0000h	00AFh (175d)	
S/W Reset	0000h	00AFh (175d)	0083h (132d)
H/W Reset	0000h	00AFh (175d)	

Flow Chart

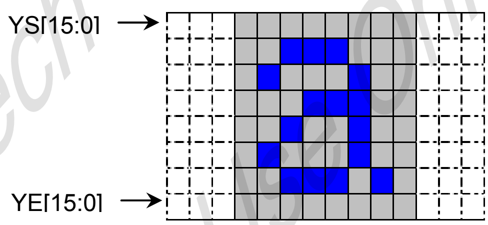


Note: B=17

6.2.21. RASET (2BH): Row Address Set

2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2BH)
1st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	00h
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	00h
3rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to define area of frame memory where MCU can access. -This command makes no change on the other driver status. -The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes. -Each value represents one column line in the Frame Memory. (Example) 
Restriction	YS [15:0] always must be equal to or less than YE [15:0] When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored. 1. 176x220 memory base (GM1, GM0 = "00") (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 219 (0DBh)): MV="0" If the "XS" or "XE" are large then 219d, it become 219d (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 175 (00AFh)): MV="1" If the "XS" or "XE" are large then 175d, it become 175d 2. 176x176 memory base (GM1, GM0 = "01") (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 175 (00AFh)): MV="0" If the "XS" or "XE" are large then 175d, it become 175d (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 175 (00AFh)): MV="1" If the "XS" or "XE" are large then 175d, it become 175d 3. 176x132 memory base (GM1, GM0 = "11") (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 131 (0083h)): MV="0" If the "XS" or "XE" are large then 131d, it become 131d (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 175 (00AFh)): MV="1" If the "XS" or "XE" are large then 175d, it become 175d
Register Availability	see table below

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176x220 memory base (GM1, GM0 = "00")

Status	Default Value		
	YS [15:0]	YE [15:0] (MV='**0**')	YE [15:0] (MV='**1**')
Power On Sequence	0000h	0DBh (219d)	
S/W Reset		0DBh (219d)	00AFh (175d)
H/W Reset		0DBh (219d)	

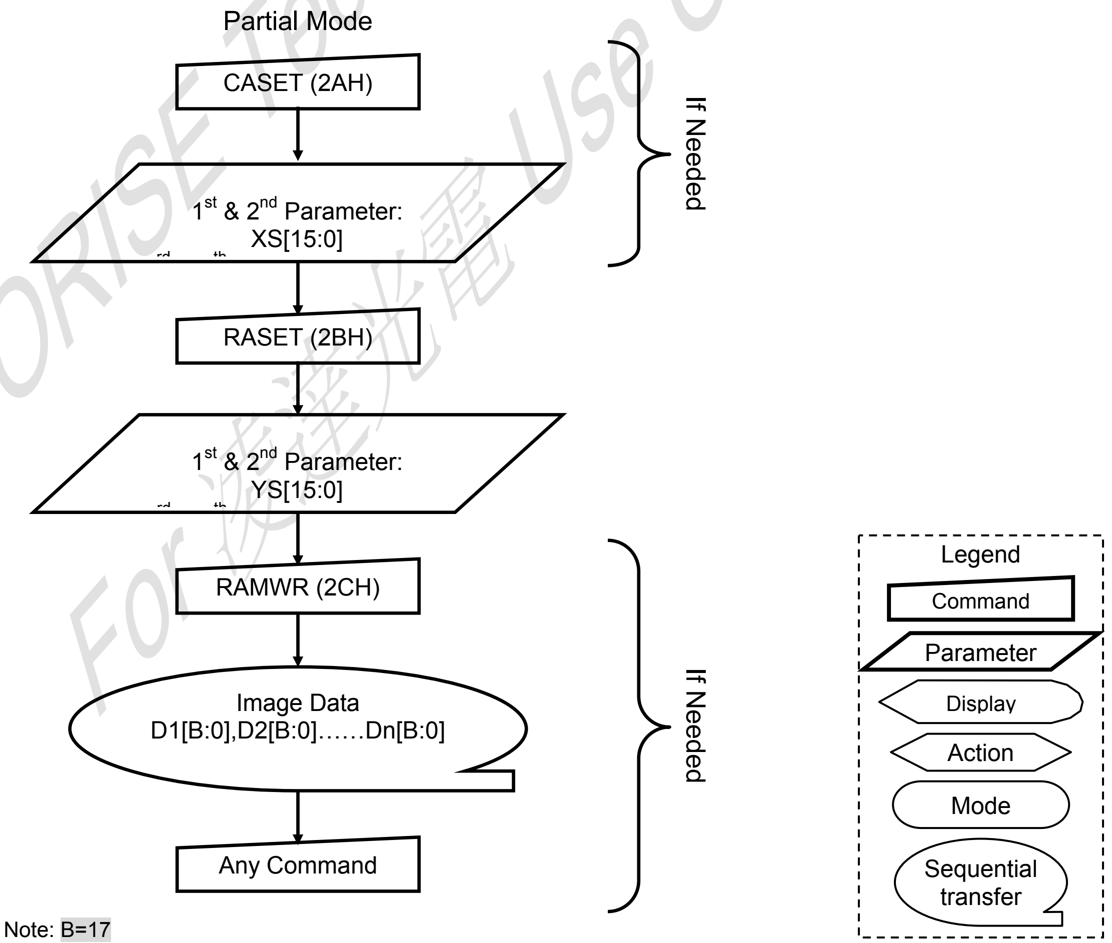
2. 176x176 memory base (GM1, GM0 = "01")

Status	Default Value		
	YS [15:0]	YE [15:0] (MV='**0**')	YE [15:0] (MV='**1**')
Power On Sequence	0000h	00AFh (175d)	
S/W Reset			
H/W Reset			

3. 176x132 memory base (GM1, GM0 = "11")

Status	Default Value		
	YS [15:0]	YE [15:0] (MV='**0**')	YE [15:0] (MV='**1**')
Power On Sequence	0000h	0083h (131d)	
S/W Reset		0083h (131d)	00AFh (175d)
H/W Reset		0083h (131d)	

Flow Chart



Note: B=17

6.2.22. RAMWR (2CH): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2CH)
1st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
|	1	↑	1	|	|	|	|	|	|	|	|	|	|
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to transfer data from MCU to frame memory. -This command makes no change to the other driver status. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTR setting. (See section 6.6) -Then D[B:0] is stored in frame memory and the column register and the row register incremented as section 6.5.2. -Sending any other command can stop Frame Write.
Restriction	In all color modes, there is no restriction on length of parameters. 1. 176x220 memory base (GM1, GM0 = "00") 176x220x18-bits memory can be written by this command Memory range: (0000h,0000h) -> (00AFh, 00DBh) 2. 176x176 memory base (GM1, GM0 = "01") 176x220x18-bits memory can be written by this command Memory range: (0000h,0000h) -> (00AFh, 00AFh) 3. 176x132 memory base (GM1, GM0 = "11") 176x220x18-bits memory can be written by this command Memory range: (0000h,0000h) -> (00AFh, 0083h)
Register Availability	(see table below)
Default	(see table below)

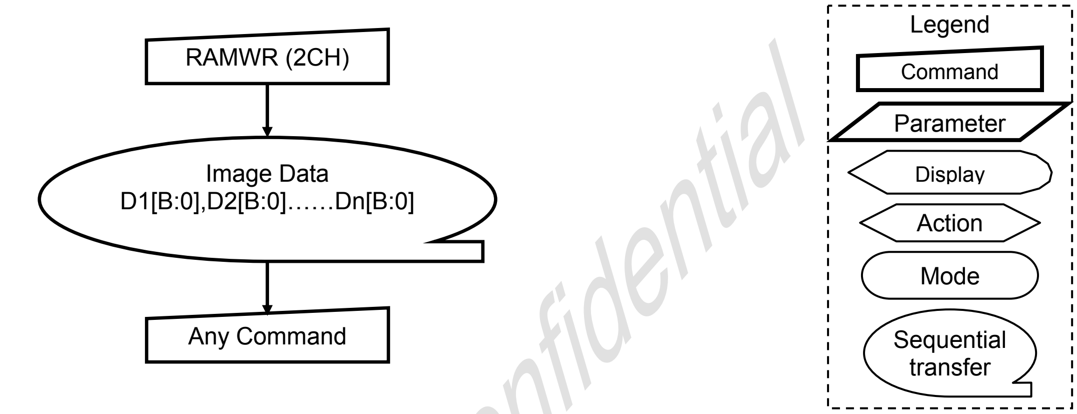
Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



Note: B=17

6.2.23. RGBSET (2DH): Colour Setting

2DH	RGBSET (Colour Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2DH)
1st Parameter	1	↑	1	-	R007	R006	R005	R004	R003	R002	R001	R000	-
|	1	↑	1	-	:	:	:	:	:	:	:	:	-
|	1	↑	1	-	Raa7	Raa6	Raa5	Raa4	Raa3	Raa2	Raa1	Raa0	-
|	1	↑	1	-	G007	G006	005	G004	G003	G002	G001	G000	-
|	1	↑	1	-	:	:	:	:	:	:	:	:	-
|	1	↑	1	-	Gbb7	Gbb6	Gbb5	Gbb4	Gbb3	Gbb2	Gbb1	Gbb0	-
|	1	↑	1	-	B007	B006	B005	B004	B003	B002	B001	B000	-
|	1	↑	1	-	:	:	:	:	:	:	:	:	-
nnd Parameter	1	↑	1	-	Bcc7	Bcc6	Bcc5	Bcc4	Bcc3	Bcc2	Bcc1	Bcc0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to define the LUT for 12-bits-to-18-bits / 16bits-to-18-bits colors depth conversations. -262K-colors used. -LUT has total trough 128 parameters. -In this condition, 4K-color (4-4-4) and 65K-color(5-6-5) data input are transferred 6(R)-6(G)-6(B) through RGB LUT table. (aa=31, bb=63, cc=31) -This command has no effect on other commands/parameters and Contents of frame memory. -Visible change takes effect next time the Frame Memory is written .
Restriction	Do not send any command before the last data is sent or LUT is not defined correctly.

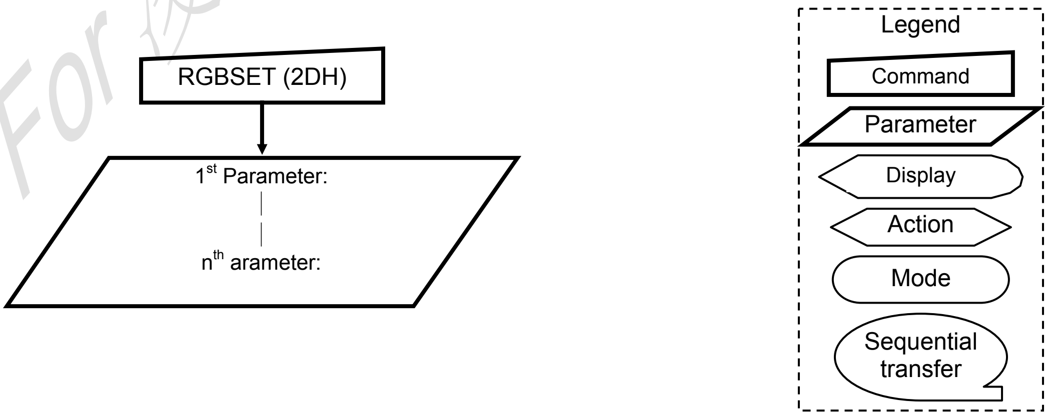
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	LUT default value
S/W Reset	Contents of the look-up table protected
H/W Reset	LUT default value

Flow Chart



6.2.24. RAMHD (2EH): Memory Read

2EH	RAMHD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2EH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
|	1	1	↑	|	|	|	|	|	|	|	|	|	|
(N+1)th Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to transfer data from frame memory to MCU. -This command makes no change to the other driver status. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTR setting. (See section 6.7) -Then D[B:0] is read back from the frame memory and the column register and the row register incremented as section 6.5.2. -Frame Read can be canceled by sending any other command. -See section 6.4 "Data color coding" for color coding (18-bits cases), when there is used 12, 16, and 18-bits data lines for image data.
Restriction	-In all color modes, the Frame Read is always 18-bits and there is no restriction on length of parameters. -Memory read is only possible via the SPI and parallel interface.

Register Availability

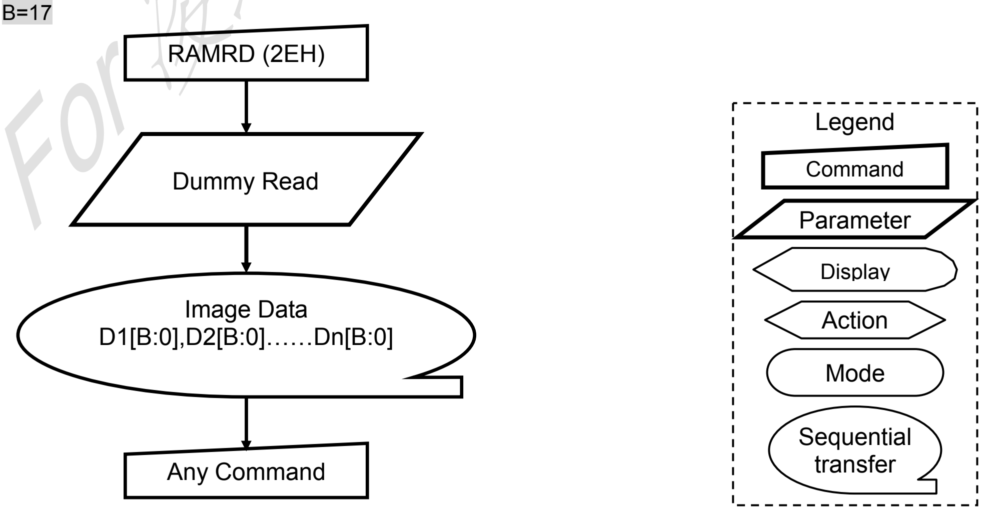
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart

Note: B=17



6.2.25. PTLAR (30H): Partial Area

30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30H)
1st Parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	00h
2nd Parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	00h
3rd Parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4th Parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

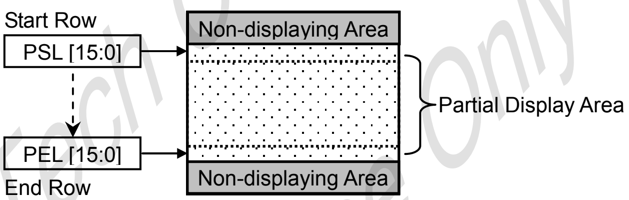
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

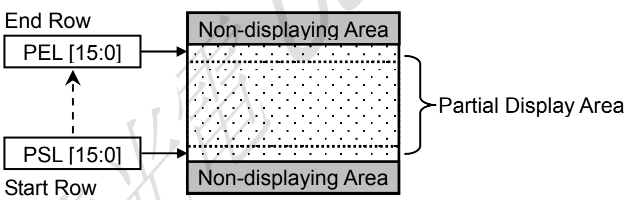
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

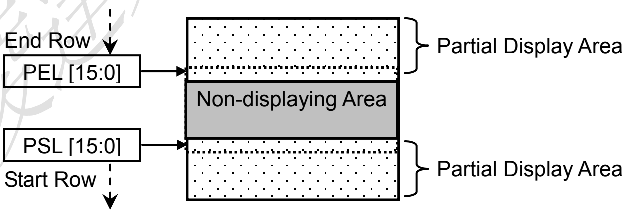
-If End Row > Start Row, when MADCTL ML='0'



-If End Row > Start Row, when MADCTL ML='1'

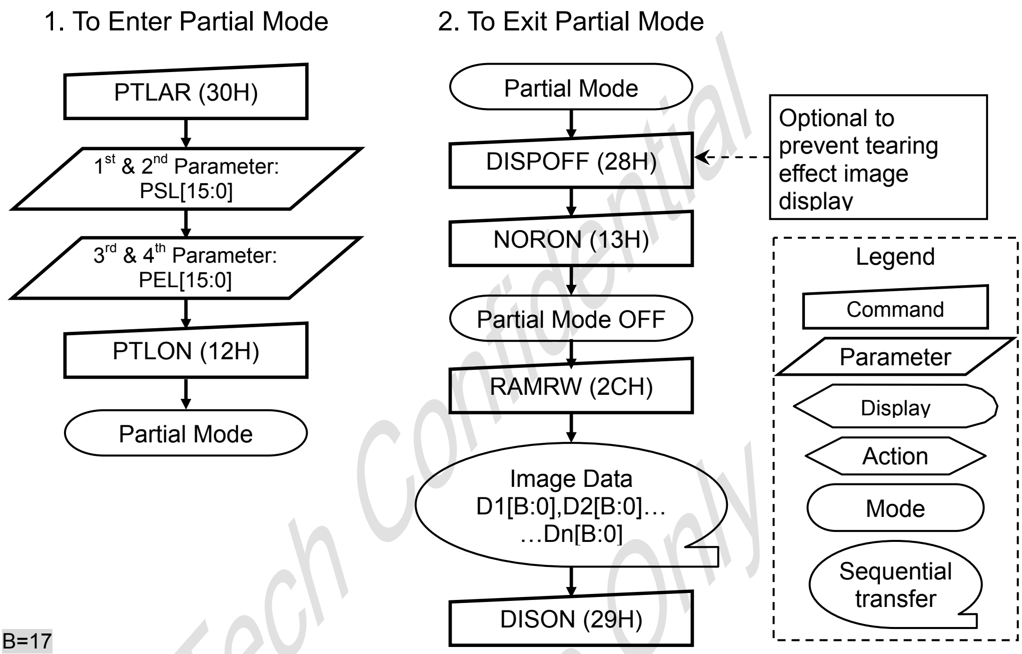


-If End Row < Start Row, when MADCTL ML='0'



-If End Row = Start Row then the Partial Area will be one row deep.

<table>
<tr><td>Restriction</td><td>-PEL [15:0] always must be equal to or less than PSL [15:0]
-When PEL [15:0] or PSL [15:0] are greater than maximum row address like below, data of out of range will be ignored.
1. 176x220 memory base (GM1, GM0 = “00”)
(Parameter range: 0 ≤ PSL [15:0] ≤ PEL [15:0] ≤ 219 (0DBh))
If the “PSL” or “PEL” are large then 219d, it become 219d
2. 176x176 memory base (GM1, GM0 = “01”)
(Parameter range: 0 ≤ PSL [15:0] ≤ PEL [15:0] ≤ 176 (00AFh))
If the “PSL” or “PEL” are large then 176d, it become 176d
3. 176x132 memory base (GM1, GM0 = “11”)
(Parameter range: 0 ≤ PSL [15:0] ≤ PEL [15:0] ≤ 131 (0083h))
If the “PSL” or “PEL” are large then 131d, it become 131d</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
1. 176x220 memory base (GM1, GM0 = “00”)
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>PSL [15:0]</th><th>PEL [15:0]</th></tr>
<tr><td>Power On Sequence</td><td rowspan="3">0000h</td><td rowspan="3">00DBh</td></tr>
<tr><td>S/W Reset</td></tr>
<tr><td>H/W Reset</td></tr>
</table>
2. 176x176 memory base (GM1, GM0 = “01”)
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>PSL [15:0]</th><th>PEL [15:0]</th></tr>
<tr><td>Power On Sequence</td><td rowspan="3">0000h</td><td rowspan="3">00AFh</td></tr>
<tr><td>S/W Reset</td></tr>
<tr><td>H/W Reset</td></tr>
</table>
3. 176x132 memory base (GM1, GM0 = “11”)
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>PSL [15:0]</th><th>PEL [15:0]</th></tr>
<tr><td>Power On Sequence</td><td rowspan="3">0000h</td><td rowspan="3">0083h</td></tr>
<tr><td>S/W Reset</td></tr>
<tr><td>H/W Reset</td></tr>
</table>
</td></tr>
</table>

Flow Chart	 Note: B=17

6.2.26. SCRLAR (33H): Scroll Area

33H	SCRLAR (Scroll Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SCRLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33H)
1st Parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	00h
2nd Parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	00h
3rd Parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	
4th Parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
5th Parameter	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	00h
6th Parameter	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	00h

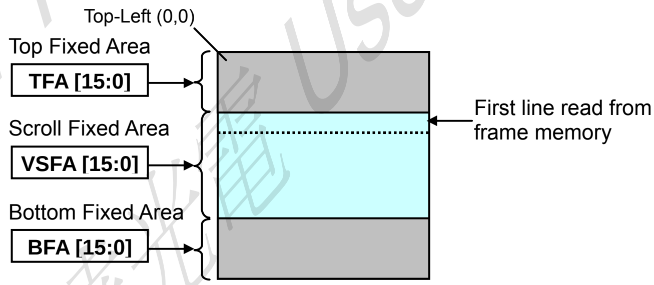
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command defines the Vertical Scrolling Area of the display.

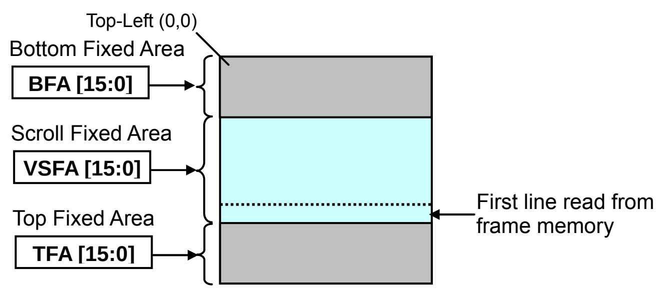
-When MADCTR ML=0

- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the bottom most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
- TFA, VSA and BFA refer to the Frame Memory row address.



-When MADCTR ML=1

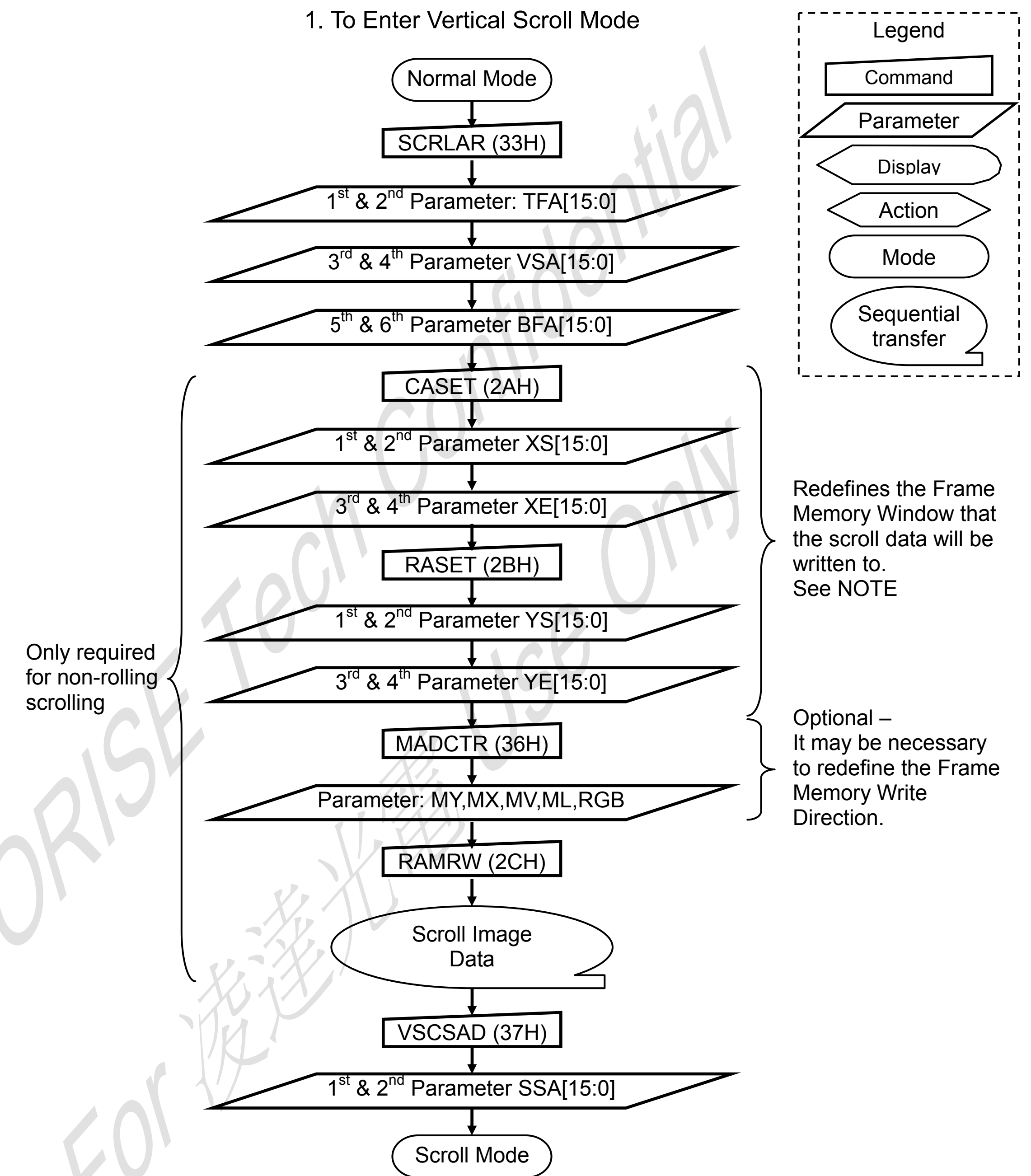
- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the top most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



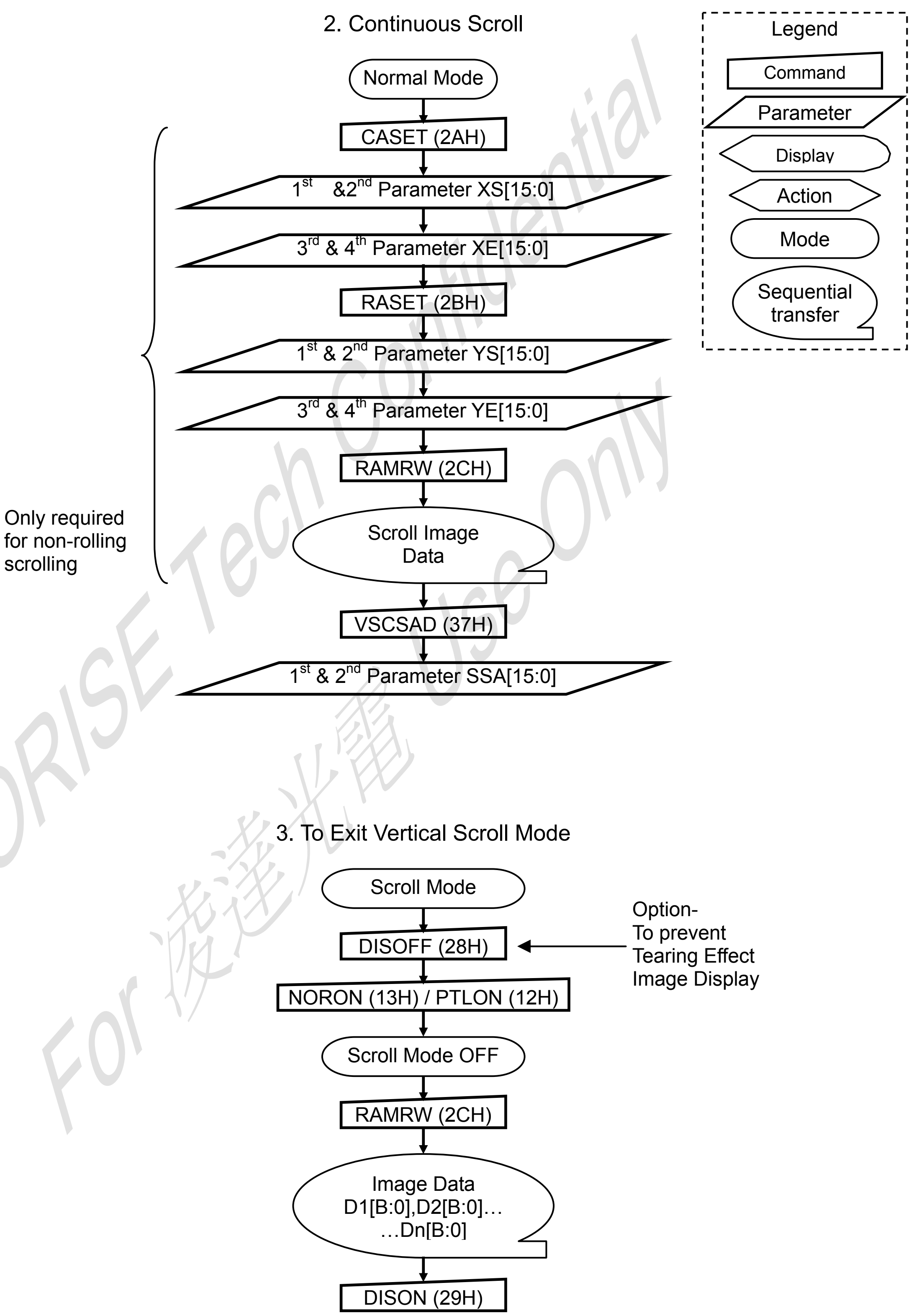
-See Section 6.5.4 for details of the Memory to Display Mapping.

<table>
<tr><td>Restriction</td><td>1. 176x220 memory base (GM1, GM0 = "00")
-The condition is 0 ≤ (TFA+VSA+BFA) ≤ 220, otherwise Scrolling mode is undefined.
2. 176x176 memory base (GM1, GM0 = "01")
-The condition is 0 ≤ (TFA+VSA+BFA) ≤ 176, otherwise Scrolling mode is undefined.
3. 176x132 memory base (GM1, GM0 = "11")
-The condition is 0 ≤ (TFA+VSA+BFA) ≤ 132, otherwise Scrolling mode is undefined.
-In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'-this only affects the Frame Memory Write.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
1. 176x220 memory base (GM1, GM0 = "00")
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>TFA [15:0]</th><th>VSA [15:0]</th><th>BFA [15:0]</th></tr>
<tr><td>Power On Sequence</td><td rowspan="3">0000h</td><td rowspan="3">00DCh</td><td rowspan="3">0000h</td></tr>
<tr><td>S/W Reset</td></tr>
<tr><td>H/W Reset</td></tr>
</table>
2. 176x176 memory base (GM1, GM0 = "01")
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>TFA [15:0]</th><th>VSA [15:0]</th><th>BFA [15:0]</th></tr>
<tr><td>Power On Sequence</td><td rowspan="3">0000h</td><td rowspan="3">00B0h</td><td rowspan="3">0000h</td></tr>
<tr><td>S/W Reset</td></tr>
<tr><td>H/W Reset</td></tr>
</table>
3. 176x132 memory base (GM1, GM0 = "11")
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>TFA [15:0]</th><th>VSA [15:0]</th><th>BFA [15:0]</th></tr>
<tr><td>Power On Sequence</td><td rowspan="3">0000h</td><td rowspan="3">0084h</td><td rowspan="3">0000h</td></tr>
<tr><td>S/W Reset</td></tr>
<tr><td>H/W Reset</td></tr>
</table>
</td></tr>
</table>

Flow Chart



NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart	 *Note: B=17* *Note: Scroll Mode can be exit by both the Normal Display Mode On (13H) and Partial Mode On (12H) commands.*

6.2.27. TEOFF (34H): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	-This command has no effect when Tearing Effect output is already OFF.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM1, RCM0 = "00", "1x"	RCM1, RCM0 = "01"
Power On Sequence	OFF	ON
S/W Reset	OFF	ON
H/W Reset	OFF	ON

Flow Chart

6.2.28. TEON (35H): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35H)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	TELOM	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

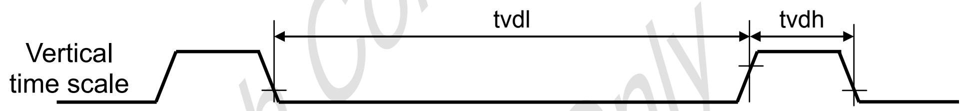
-This command is used to turn ON the Tearing Effect output signal from the TE signal line.

-This output is not affected by changing MADCTR bit ML.

-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).

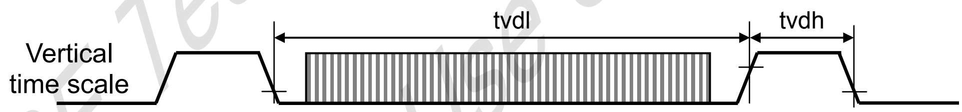
—When M='0':

The Tearing Effect Output line consists of V-Blanking information only.



—When M='1':

The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

-This command has no effect when Tearing Effect output is already OFF.

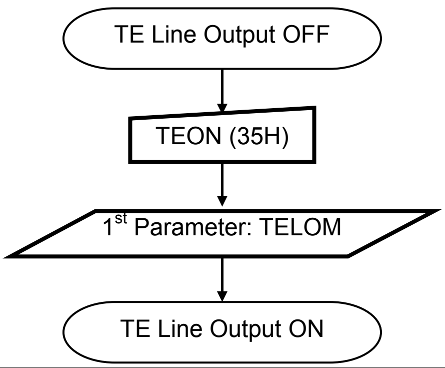
Register Availability

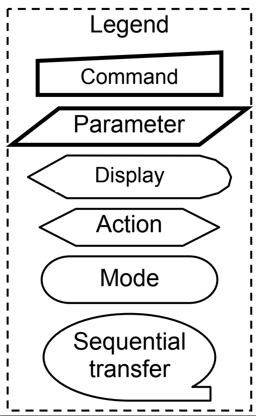
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM1, RCM0 = "00", "1x"	RCM1, RCM0 = "01"
Power On Sequence	OFF & TELOM=0	ON & TELOM=0
S/W Reset	OFF & TELOM=0	ON & TELOM=0
H/W Reset	OFF & TELOM=0	ON & TELOM=0

Flow Chart





6.2.29. MADCTR (36H): Memory Data Access Control

36H	MADCTR (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTR	0	↑	1	-	0	0	1	1	0	1	1	0	(36H)
1st Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

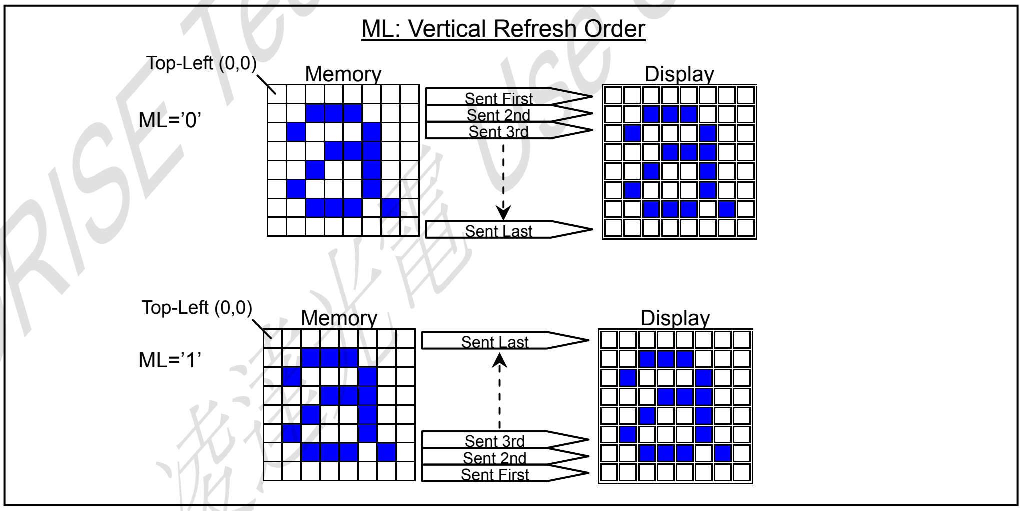
Description

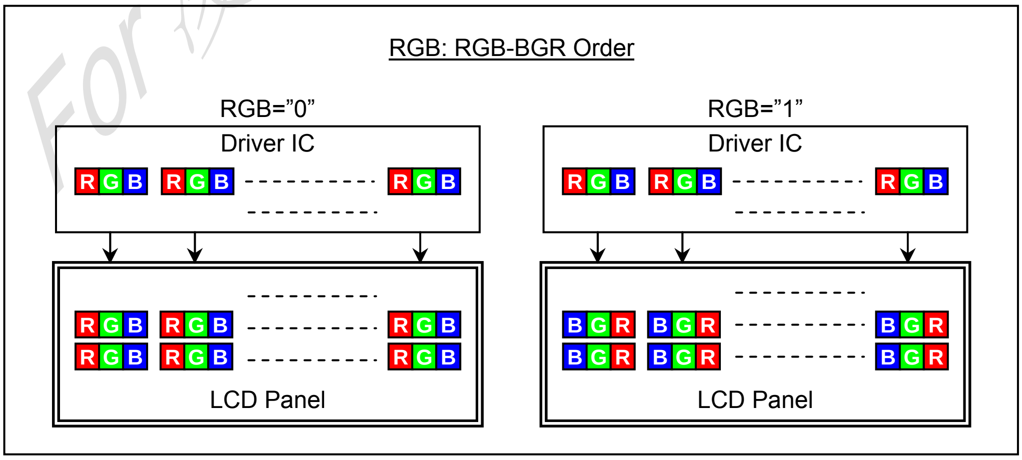
-This command defines read/ write scanning direction of frame memory.

-This command makes no change on the other driver status.

-Bit Assignment

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction. (See Section 8.11)
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)





Restriction

D1 and D0 of the 1st parameter are set to "00" internally.

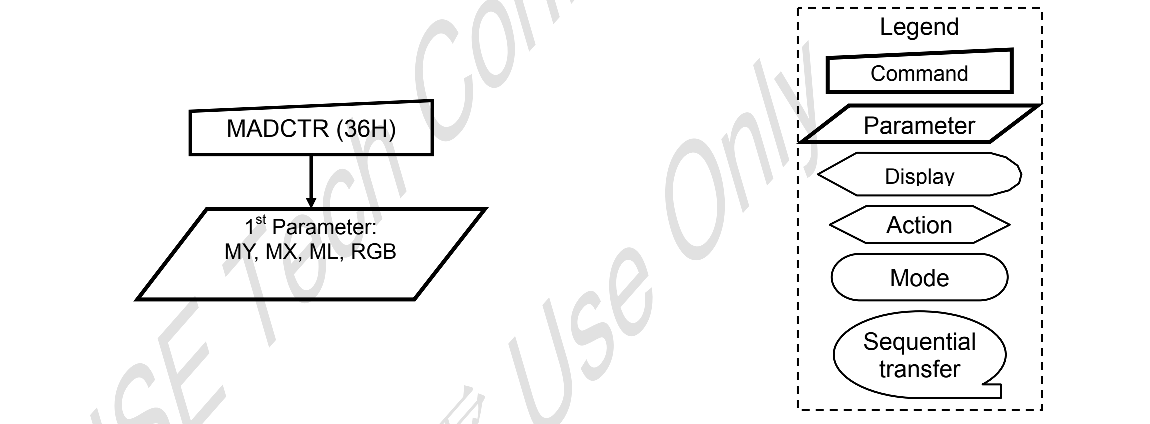
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,

Flow Chart



6.2.30. VSCSAD (37H): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1st Parameter	1	↑	1	-	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	
2nd Parameter	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

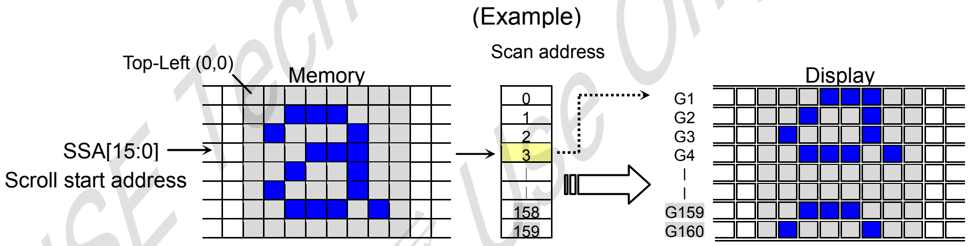
-This command Start the scrolling.

-Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTR ML= '0'

Example:

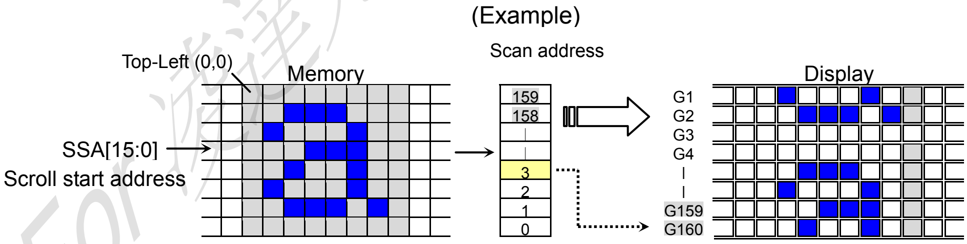
—When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=220 and Vertical Scrolling Pointer SSA= '3'.



When MADCTR ML = '1'

Example:

—When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=220 and SSA= '3'



NOTE: -When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
-SSA refers to the Frame Memory scan address.

Restriction

-Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.

SSA[15:0] is based on 1-line unit.

-SSA[15:0] = 0000h, 0001h, 0002h, 0003h, … , 00A1h

<table>
<tr><td>Register Availability</td><td>

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

</td></tr>
<tr><td>Default</td><td>

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.31. IDMOFF (38H): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to recover from Idle mode on. -There will be no abnormal visible effect on the display mode change transition. -In the idle off mode, 1. LCD can display 4k, 65k and 262k -colors. 2. Normal frame frequency is applied.
Restriction	-This command has no effect when module is already in idle off mode.
Register Availability	(see table below)
Default	(see table below)
Flow Chart	(see chart below)

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart

6.2.32. IDMON (39H): Idle Mode On

39H	IDMON (Idle Mode On)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39H)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

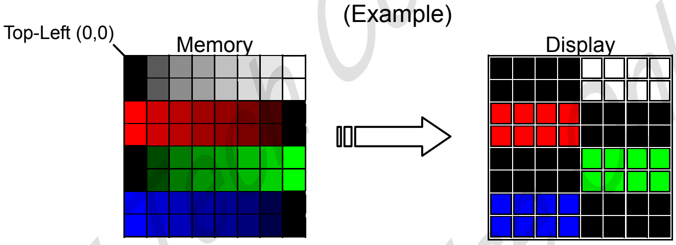
-This command is used to enter into Idle mode on.

-There will be no abnormal visible effect on the display mode change transition.

-In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38H) command

(Example)



"x" Don't care

Color	$R_5 R_4 R_3 R_2 R_1 R_0$	$G_5 G_4 G_3 G_2 G_1 G_0$	$B_5 B_4 B_3 B_4 B_1 B_0$
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Restriction

This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart	 Idle mode OFF IDMOFF (39) Idle mode ON Legend Command Parameter Display Action Mode Sequential transfer

6.2.33. COLMOD (3AH): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3AH)
1st Parameter	1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface and RGB interface. The formats are shown in the table:

IFPF[2:0]		MCU Interface Color Format
011	3	12-bits/pixel
101	5	16-bits/pixel
110	**6**	**18-bits/pixel**
111	7	Reserved

Others are no define and invalid

VIPF[3:0]		RGB Interface Color Format
0101	5	16-bits/pixel (1-times data transfer)
0110	**6**	**18-bits/pixel (1-times data transfer)**
0111	7	Reserved
1110	14	18-bits/pixel (3-times data transfer)

Others are no define and invalid

Note1: In 12-bits/Pixel, 16-bits/Pixel or 18-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.
Note2: When RGB I/F the 12-bit/pixel don't care
Note 3: When VIPF[3:0]="1110",6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

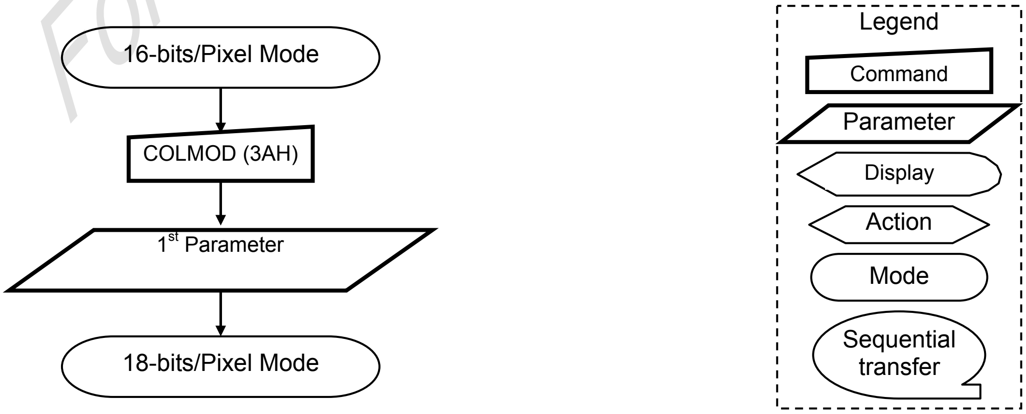
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	IFPF[2:0]	VIPF[3:0]
Power On Sequence	0101 (16-bits/pixel)	0110 (18-bits/pixel)
S/W Reset	No Change	No Change
H/W Reset	0101 (16-bits/pixel)	0110 (18-bits/pixel)

Flow Chart

Example:



6.2.34. RDID1 (DAH): Read ID1 Value

DAH	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This read byte returns 8-bits LCD module's manufacturer ID -The 1st parameter is dummy data -The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. *NOTE: See command RDDID (04H), 2nd parameter.*
Restriction	
Register Availability	see table below
Default	see table below
Flow Chart	see figure below

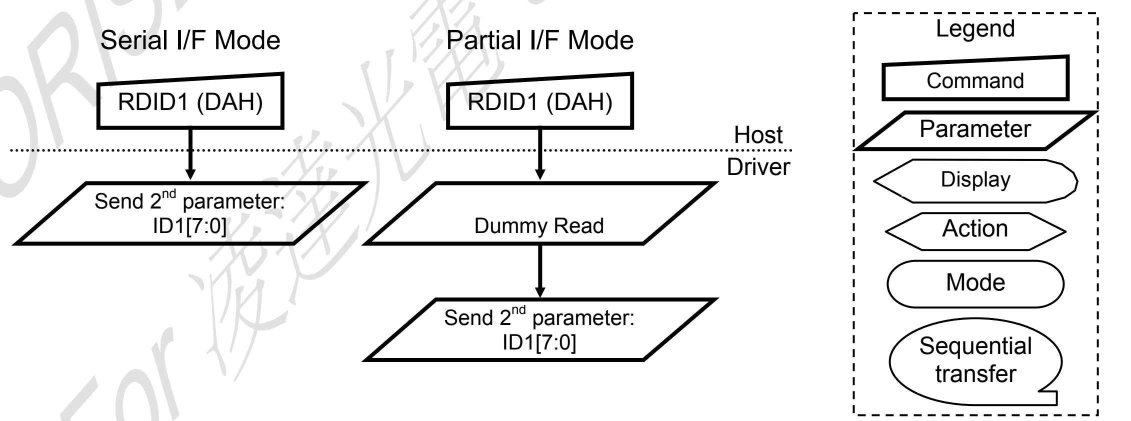
Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	38h
S/W Reset	38h
H/W Reset	38h

Flow Chart:



6.2.35. RDID2 (DBH): Read ID2 Value

DBH	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This read byte returns 8-bits LCD module/driver version ID -The 1st parameter is dummy data -The 2nd parameter (ID26 to ID20): LCD module/driver version ID *NOTE: See command RDDID (04H), 3rd parameter.*
Restriction	

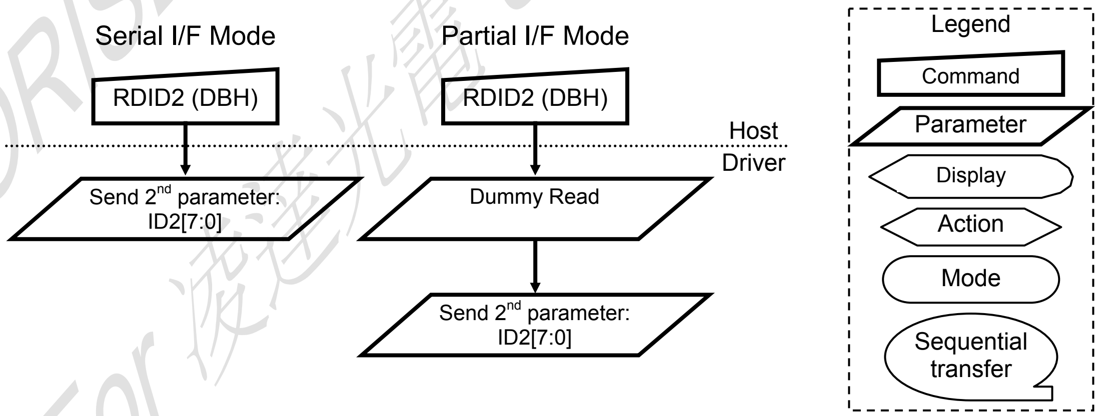
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

Flow Chart



6.2.36. RDID3 (DCH): Read ID3 Value

DCH	RDID3 (Read ID2 Value)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCH)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	62h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This read byte returns 8-bits LCD module/driver ID. -The 1st parameter is dummy data -The 2nd parameter (ID37 to ID30): LCD module/driver ID. *NOTE: See command RDDID (04H), 4th parameter.*
Restriction	-

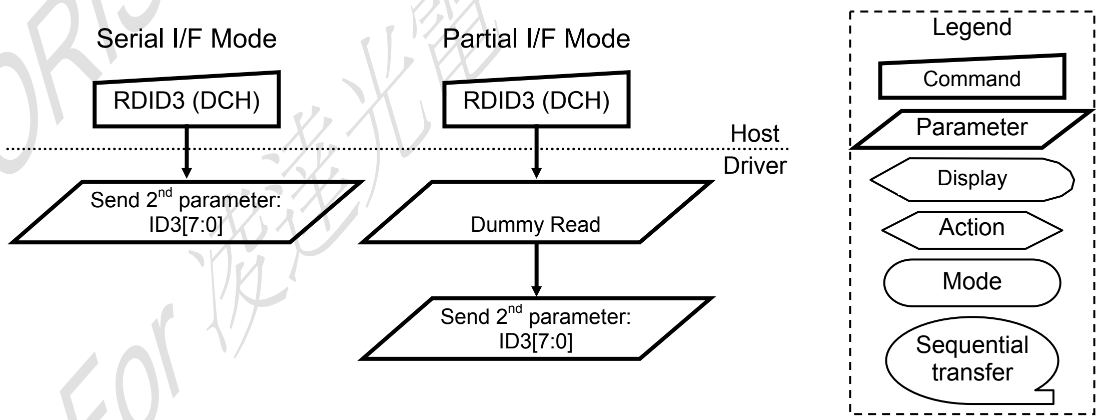
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	62h
S/W Reset	62h
H/W Reset	62h

Flow Chart



6.2.37. SRGBOFF (AAH): Separate RGB Gamma OFF

AAH	SRGBOFF (Separate RGB Gamma OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SRGBOFF	0	↑	1	-	1	0	1	0	1	0	1	0	(AAH)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to turn OFF the separate RGB gamma function.
Restriction	-This command has no effect when separate RGB gamma function OFF.

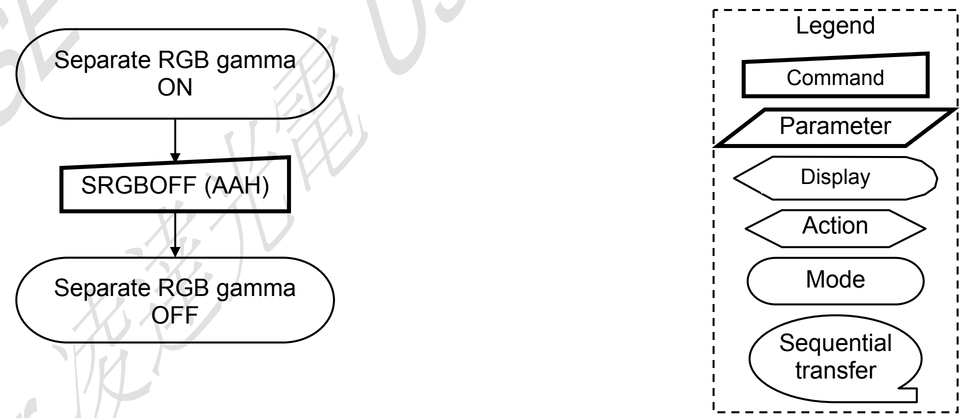
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM1, RCM0 = "00", "1x"	RCM1, RCM0 = "01"
Power On Sequence	OFF	ON
S/W Reset	OFF	ON
H/W Reset	OFF	ON

Flow Chart



6.2.38. SRGBOFF (ABH): Separate RGB Gamma ON

ABH	SRGBOFF (Separate RGB Gamma ON)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SRGBON	0	↑	1	-	1	0	1	0	1	0	1	1	(ABH)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to turn On the separate RGB gamma function.
-In this mode, It only the gamma curve 2.2 (GC0) can be separated to R, G, and B gamma curve

Restriction

-This command has no effect when separate RGB gamma function ON.

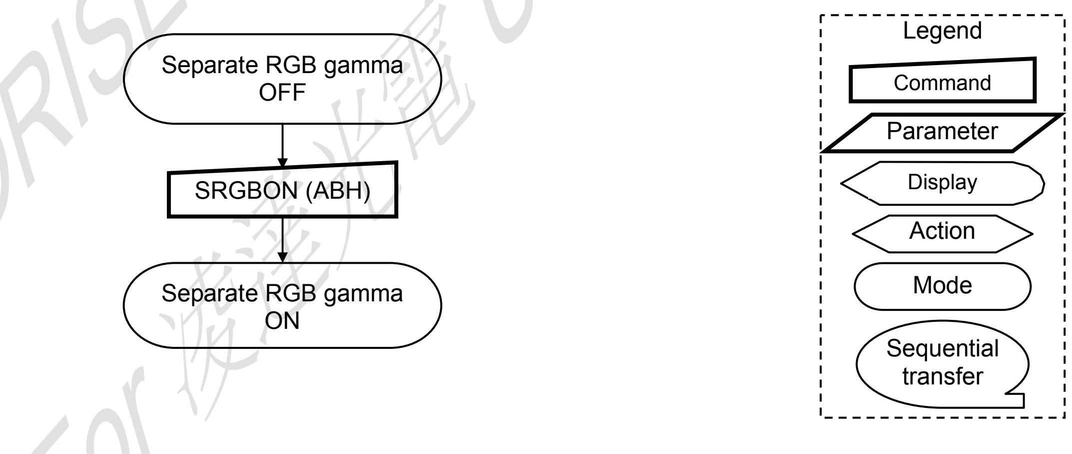
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM1, RCM0 = "00", "1x"	RCM1, RCM0 = "01"
Power On Sequence	OFF	ON
S/W Reset	OFF	ON
H/W Reset	OFF	ON

Flow Chart



6.2.39. VSYNCOFF (ACH): VSYNC Interface OFF

ACH	VSYNCOFF (VSYNC Interface OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSYNCOFF	0	↑	1	-	1	0	1	0	1	1	0	0	(ACH)
1st Parameter	No Parameter												--

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to turn OFF the VSYNC interface function.
Restriction	-This command has no effect when VSYNC interface OFF. -Input Vs signal for more than 1 frame period after turn OFF the VSYNC I/F

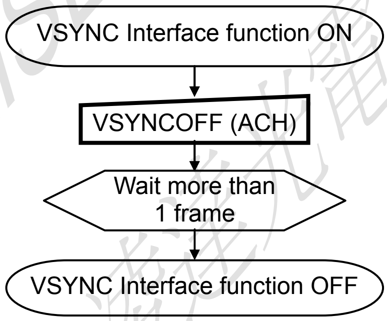
Register Availability

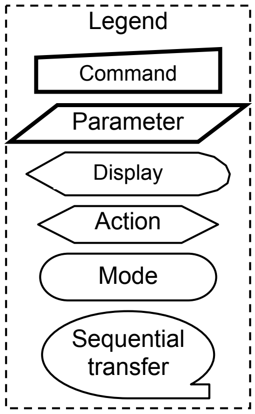
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM1, RCM0 = "00", "1x"	RCM1, RCM0 = "01"
Power On Sequence	OFF	ON
S/W Reset	OFF	ON
H/W Reset	OFF	ON

Flow Chart





Input Vs signal foe more than 1 frame period after turn OFF the VSYNC I/F

6.2.40. VSYNCON (ADH): VSYNC Interface ON

ADH	VSYNCOFF (VSYNC Interface ON)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSYNCON	0	↑	1	-	1	0	1	0	1	1	0	1	(ADH)
1st Parameter	No Parameter												--

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to turn ON the VSYNC interface function.
Restriction	-This command has no effect when VSYNC interface ON. -Input VS signal before turn On the VSYNC I/F
Register Availability	(see table below)
Default	(see table below)
Flow Chart	(see chart below)

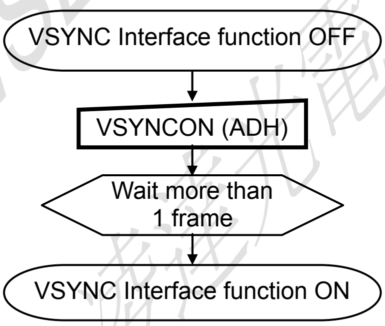
Register Availability

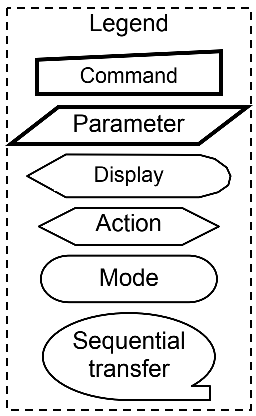
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM1, RCM0 = "00", "1x"	RCM1, RCM0 = "01"
Power On Sequence	OFF	ON
S/W Reset	OFF	ON
H/W Reset	OFF	ON

Flow Chart





Note: Input VS signal before turn On the VSYNC I/F

6.2.41. VSCTR1 (AEH): VSYNC Interface function control 1

AEH	VSYNCTR1 (VSYNC Interface function control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCTR1	0	↑	1	-	1	0	1	0	1	1	0	1	(AEH)
1st Parameter	1	↑	1	-	VSFP3	VSFP2	VSFP1	VSFP0	VSBP3	VSBP2	VSBP1	VSBP0	2Eh

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the back porch and front porch on the VSYNC interface. The setting becomes effective as soon as the command is received.

-VSFP: Front porch set on VSYNC I/F

-VSBP: Back porch set on VSYNC I/F

VSBP[3:0] VSFP[3:0]		Front porch period (Line)	Back porch period (Line)
0000	0	Setting inhibited	Setting inhibited
0001	1	Setting inhibited	Setting inhibited
0010	2	2-lines	2-lines
0011	3	3-lines	3-lines
0100	4	4-lines	4-lines
0101	5	5-lines	5-lines
0110	6	6-lines	6-lines
0111	7	7-lines	7-lines
1000	8	8-lines	8-lines
1001	9	9-lines	9-lines
1010	10	10-lines	10-lines
1011	11	11-lines	11-lines
1100	12	12-lines	12-lines
1101	13	13-lines	13-lines
1110	14	14-lines	14-lines
1111	15	Setting inhibited	Setting inhibited

Restriction

-The command is enabled by VSYNCON (ADH)

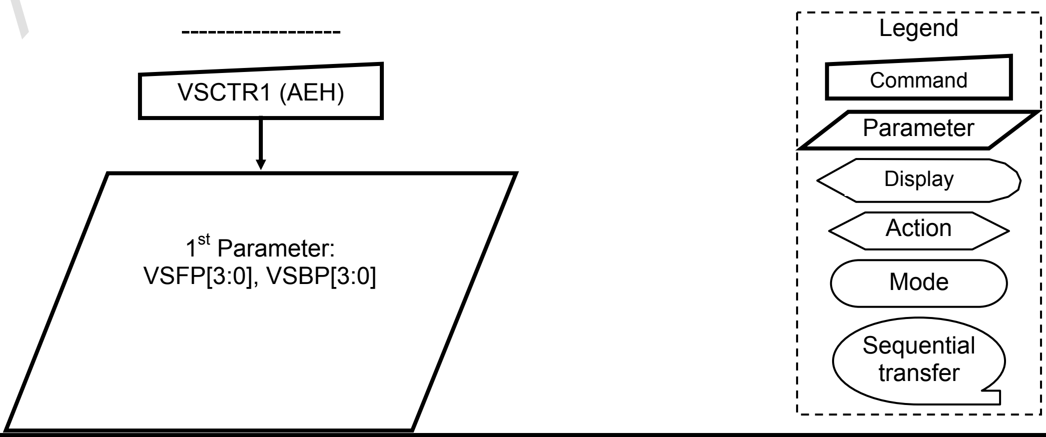
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VSFP[3:0]	VSBP[3:0]
Power On Sequence	2d	14d
S/W Reset	No Change	No Change
H/W Reset	2d	14d

Flow Chart



6.3. Panel Command Description

6.3.1. RGBCTR (B0H): RGB signal control

B0H	RGBCTR (RGB signal control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBCTR	0	↑	1	-	1	0	1	1	0	0	0	0	(B0H)
1st Parameter	1	↑	1	-	0	0	0	ICM	DP	EP	HSP	VSP	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the operation status on the RGB interface. The setting becomes effective as soon as the command is received.

-ICM: GRAM Write/Read frequency and data input select on the RGB interface

ICM	Write/ Read frequency and input data select		
	Write cycle	Read cycle	Data input
0	PCLK	PCLK	D[B:0]
1	SCL	Internal oscillator	SDA

B=17

Symbol	Name	Clock polarity set for RGB Interface
DP	PCLK polarity set	'1' = data fetched at the falling edge '0' = data fetched at the rising edge
EP	Enable polarity set	'1' = Low enable for RGB interface '0' = High enable for RGB interface
HSP	Hsync polarity set	'1' = High level sync clock '0' = Low level sync clock
VSP	Vsync polarity set	'1' = High level sync clock '0' = Low level sync clock

Restriction

-If this register not using the register need be reserved.

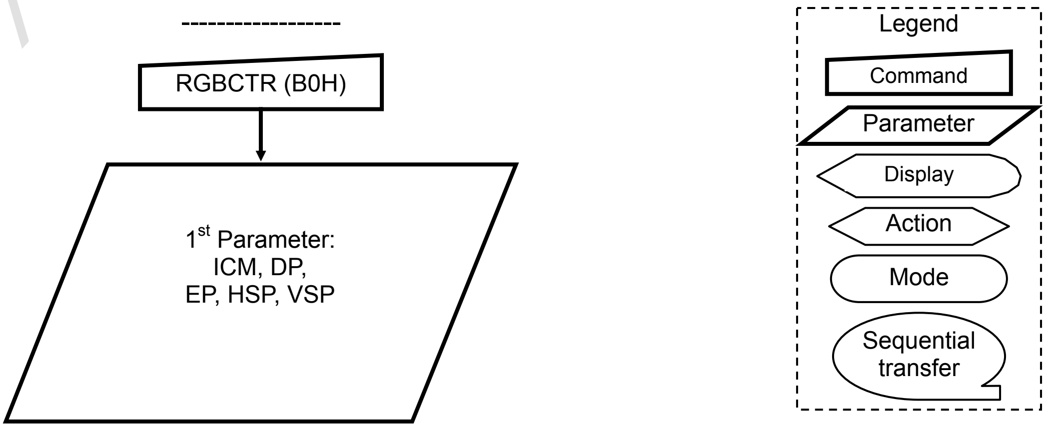
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	ICM	DP/EP/HSP/VSP
Power On Sequence	0d	0d/0d/0d/0d
S/W Reset	0d	0d/0d/0d/0d
H/W Reset	0d	0d/0d/0d/0d

Flow Chart



6.3.2. FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	FRMCTR1 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st Parameter	1	↑	1	-	0	0	0	0	FP0[3]	FP0[2]	FP0[1]	FP0[0]	-
2nd Parameter	1	↑	1	-	0	0	0	0	BP0[3]	BP0[2]	BP0[1]	BP0[0]	-
3rd Parameter	1	↑	1	-	0	0	0	0	RTN0 [3]	RTN0 [2]	RTN0 [1]	RTN0 [0]	-

NOTE: "-" Don't care

Description

-Set the frame frequency of the full colors normal mode in MPU interface.

--The default vaule of BP0, FP0, and RTN0 can fit the frame frequency to be 65Hz ±5%.

FP0[3:0]	Amount of Front Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

BP0[3:0]	Amount of Back Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

RTN0[3:0]	No. of clock in one line
0	16
1	17
2	18
3	19
4	20
…	…
D	29
E	30
F	31

Restriction

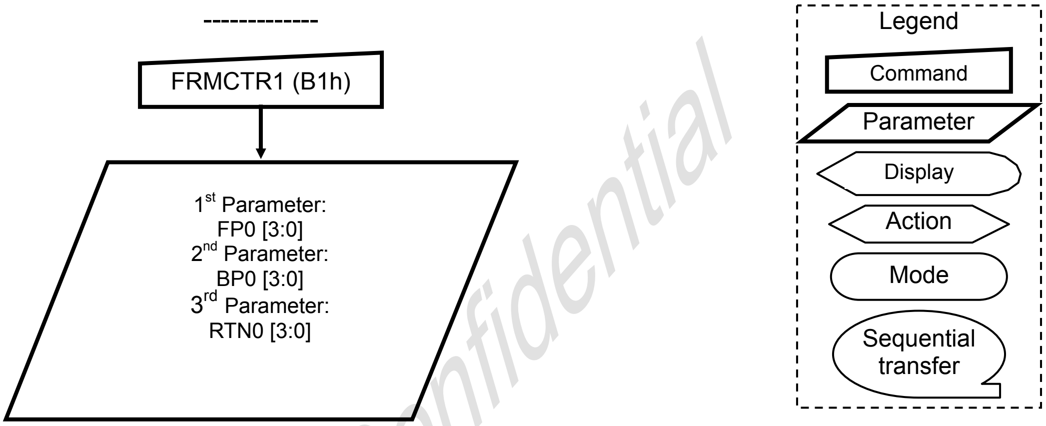
-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	FP0	BP0	RTN0
Power On Sequence	2d	14d	0d
S/W Reset	2d	14d	0d
H/W Reset	2d	14d	0d

Flow Chart	

FRMCTR1 (B1h)
1st Parameter: FP0 [3:0]
2nd Parameter: BP0 [3:0]
3rd Parameter: RTN0 [3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.3.3. FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

B2H	FRMCTR2 (Frame Rate Control)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st Parameter	1	↑	1	-	0	0	0	0	FP1[3]	FP1[2]	FP1[1]	FP1[0]	-
2nd Parameter	1	↑	1	-	0	0	0	0	BP1[3]	BP1[2]	BP1[1]	BP1[0]	-
3rd Paramete	1	↑	1	-	0	0	0	0	RTN1 [3]	RTN1 [2]	RTN1 [1]	RTN1 [0]	-

NOTE: "-" Don't care

Description

-Set the frame frequency of the Idle mode in MPU interface.

-The default vaule of BP1, FP1, and RTN1 can fit the frame frequency to be 70Hz ±5%.

FP1[3:0]	Amount of Front Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

BP1[3:0]	Amount of Back Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

RTN1[3:0]	No. of clock in one line
0	16
1	17
2	18
3	19
4	20
…	…
D	29
E	30
F	31

Restriction

-If this register not using the register need be reserved.

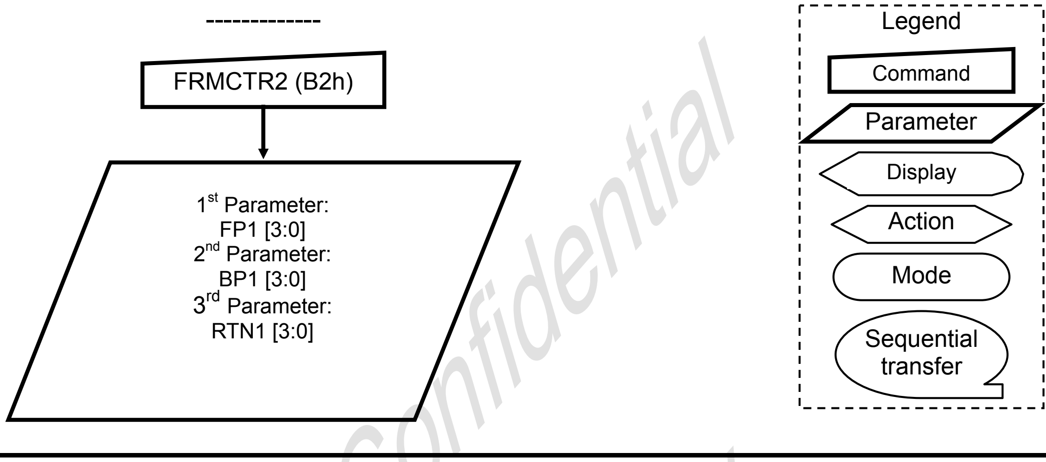
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	FP1	BP1	RTN1
Power On Sequence	2d	14d	0d
S/W Reset	2d	14d	0d
H/W Reset	2d	14d	0d

Flow Chart



FRMCTR2 (B2h)
1st Parameter:
FP1 [3:0]
2nd Parameter:
BP1 [3:0]
3rd Parameter:
RTN1 [3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

6.3.4. FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3H	FRMCTR3 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st Parameter	1	↑	1	-	0	0	0	0	FP2[3]	FP2[2]	FP2[1]	FP2[0]	-
2nd Parameter	1	↑	1	-	0	0	0	0	BP2[3]	BP2[2]	BP2[1]	BP2[0]	-
3rd Parameter	1	↑	1	-	0	0	0	0	RTN2 [3]	RTN2 [2]	RTN2 [1]	RTN2 [0]	-

NOTE: "-" Don't care

Description

-Set the frame frequency of the Partial mode/ full colors in MPU interface.

-The default vaule of BP2, FP2, and RTN2 can fit the frame frequency to be 70Hz ±5% with frame inversion and 65Hz ±5% with line inversion in this mode

FP2[3:0]	Amount of Front Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

BP2[3:0]	Amount of Back Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

RTN2[3:0]	No. of clock in one line
0	16
1	17
2	18
3	19
4	20
…	…
D	29
E	30
F	31

Restriction

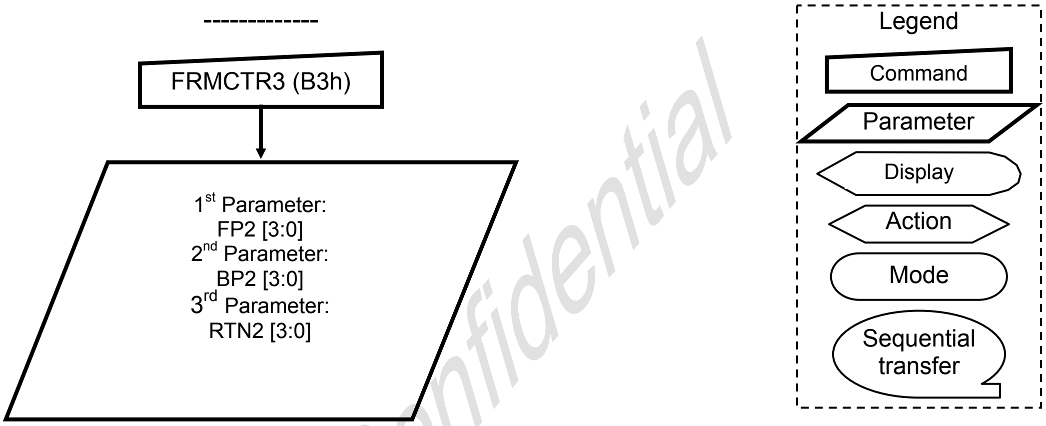
-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	FP2	BP2	RTN2
Power On Sequence	2d	14d	0d
S/W Reset	2d	14d	0d
H/W Reset	2d	14d	0d

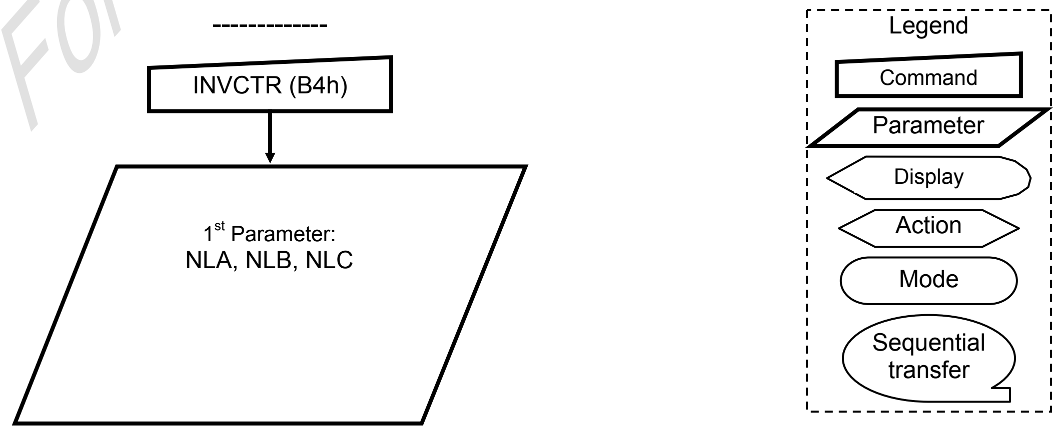
Flow Chart	

FRMCTR3 (B3h)
1st Parameter:
FP2 [3:0]
2nd Parameter:
BP2 [3:0]
3rd Parameter:
RTN2 [3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

6.3.5. INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-Display Inversion mode control -NLA: Inversion setting in full colors normal mode (Normal mode on) <table><tr><th>NLA</th><th>Inversion setting in full colours normal mode</th></tr><tr><td>0</td><td>Line Inversion</td></tr><tr><td>1</td><td>Frame Inversion</td></tr></table> -NLB: Inversion setting in Idle mode (Idle mode on) <table><tr><th>NLB</th><th>Inversion setting in Idle mode</th></tr><tr><td>0</td><td>Line Inversion</td></tr><tr><td>1</td><td>Frame Inversion</td></tr></table> -NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off) <table><tr><th>NLC</th><th>Inversion setting in full colours partial mode</th></tr><tr><td>0</td><td>Line Inversion</td></tr><tr><td>1</td><td>Frame Inversion</td></tr></table>
Restriction	-If this register not using the register need be reserved.
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr><tr><th>NLA</th><th>NLB</th><th>NLC</th><th>B4h</th></tr><tr><td>Power On Sequence</td><td>0d</td><td>1d</td><td>0d</td><td>02h</td></tr><tr><td>S/W Reset</td><td>0d</td><td>1d</td><td>0d</td><td>02h</td></tr><tr><td>H/W Reset</td><td>0d</td><td>1d</td><td>0d</td><td>02h</td></tr></table>
Flow Chart	

6.3.6. RGBBPCTR (B5h): RGB Interface Blanking Porch setting

B5H	**RGBPSET (RGB Interface Blanking Porch setting)**												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBBPCTR	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
1st Parameter	1	↑	1	-					VBP[3]	VBP[2]	VBP[1]	VBP[0]	-

NOTE: "-" Don't care

Description

-Set the blanking porch in the RGB interface

VBP[3:0]	Amount of Back Porch in RGB interface
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

Restriction

-If this register not using the register need be reserved.

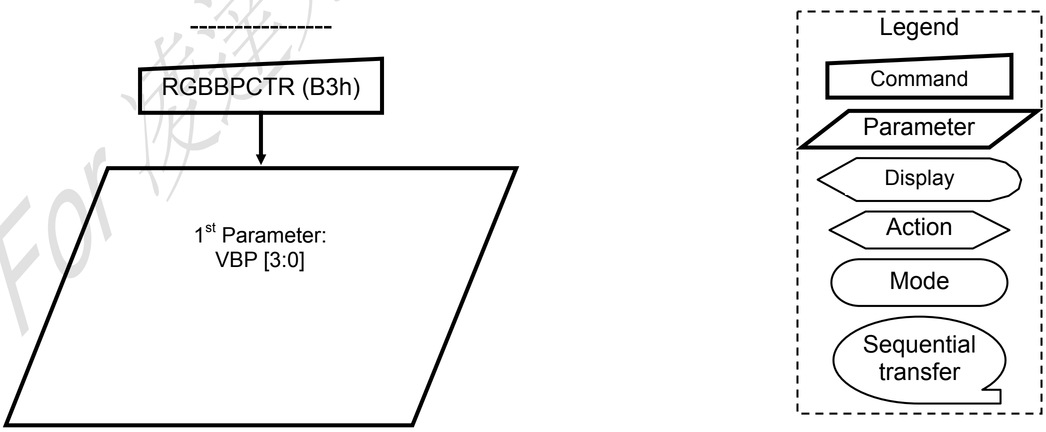
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VBP
Power On Sequence	3d
S/W Reset	3d
H/W Reset	3d

Flow Chart



6.3.7. DISSET5 (B6h): Display Function set 5

B4H	DISSET (Display Function set 5)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET5	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)
1st Parameter	1	↑	1	-	0	0	NO1	NO0	SDT1	STD0	EQ1	EQ0	
2nd Parameter	1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0	

NOTE: "-" Don't care

Description

-1st parameter: Set output waveform relation.

-NO[1:0]: Set the amount of non-overlap of the gate output

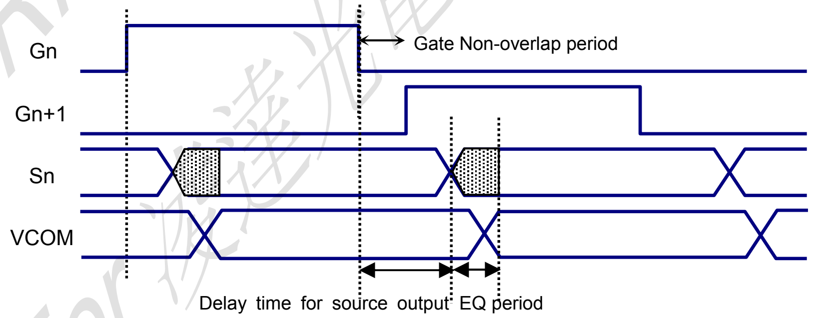
NO[1:0]		Amount of non-overlap of the gate output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	4 clock cycle
01	1	4 clock cycle	16 clock cycle
10	2	6 clock cycle	24 clock cycle
11	3	8 clock cycle	32 clock cycle

-SDT[1:0]: Set delay amount from gate signal falling edge of the source output.

SDT[1:0]		Amount of non-overlap of the source output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	4 clock cycle
01	1	2 clock cycle	8 clock cycle
10	2	3 clock cycle	12 clock cycle
11	3	4 clock cycle	16 clock cycle

-EQ[1:0]: Set the Equalizing period

EQ[1:0]		EQ period	
		Refer the Internal oscillator	Refer the PCLK
00	0	No EQ	No EQ
01	1	2 clock cycle	4 clock cycle
10	2	4 clock cycle	16 clock cycle
11	3	6 clock cycle	24 clock cycle



-2nd parameter: Set the output waveform in non-display area.

-PTG[1:0]: Determine gate output in a non-display area in the partial mode

PTG[1:0]		Gate output in a non-display area
00	0	Normal scan
01	1	Fix on VGL
10	2	Fix on VGL
11	3	Fix on VGL

-PT[1:0]: Determine Source /VCOM output in a non-display area in the partial mode

PT[1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive	Negative	Positive	Negative
00	0	V63	V0	VCOML	VCOMH
01	1	V0	V63	VCOML	VCOMH
10	2	AGND	AGND	AGND	AGND
11	3	Hi-z	Hi-z	AGND	AGND

Restriction	-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]
Power On Sequence	1d	1d	2d	0d	2d
S/W Reset	1d	1d	2d	0d	2d
H/W Reset	1d	1d	2d	0d	2d

Flow Chart

6.3.8. PWCTR1 (C0H): Power Control 1

C0H	PWCTR1 (Power Control 1)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0H)
1st Parameter	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	05h
2nd Parameter	1	↑	1	-	0	0	0	0	0	VCI2	VCI1	VCI0	05h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the GVDD and VCI1 voltage

VRH[4:0]		GVDD
00000	0	5.00
00001	1	4.75
00010	2	4.70
00011	3	4.65
00100	4	4.60
00101	**5**	**4.55**
00110	6	4.50
00111	7	4.45
01001	9	4.35
01010	10	4.30
01011	11	4.25
01100	12	4.20
01101	13	4.15
01110	14	4.10
01111	15	4.05
10000	16	4.00
10001	17	3.95
10010	18	3.90
10011	19	3.85
10100	20	3.80
10101	21	3.75
10110	22	3.70
10111	23	3.65
11000	24	3.60
11001	25	3.55
11010	26	3.50
11011	27	3.45
11100	28	3.40
11101	29	3.35
11110	30	3.25
11111	31	3.00

VC[2:0]		VCI1
000	0	2.75
001	1	2.70
010	2	2.65
011	3	2.60
100	4	2.55
101	**5**	**2.50**
110	6	2.80
111	7	2.90

Restriction

-If this register not using the register need be reserved.

-The deviation value of GVDD between with Measurement and Specification: **Max <=50mV**

-The deviation value of VCI1 between with Measurement and Specification: **Max <=2% deviation**

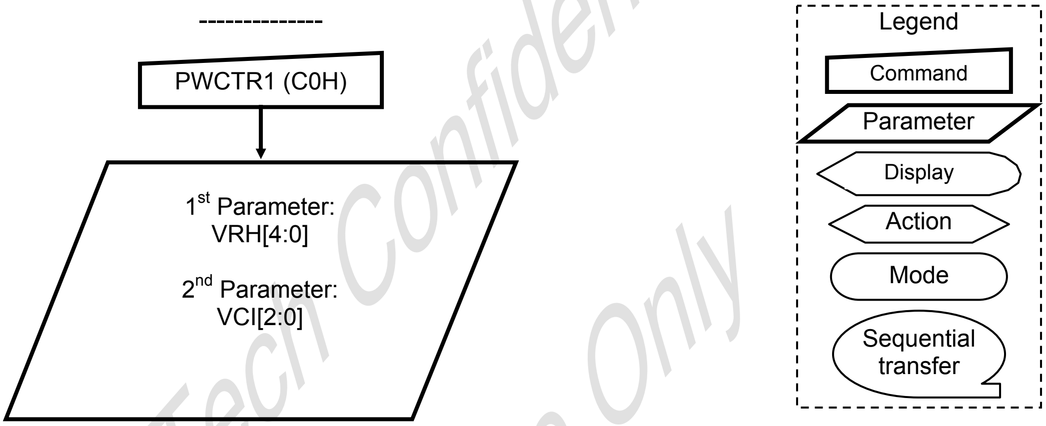
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	LCM = '01' TM LC Type		LCM = '11' ECB LC type	
	VRH[4:0]	VC[2:0]	VRH[4:0]	VC[2:0]
Power On Sequence	5d	5d	5d	5d
S/W Reset	5d	5d	5d	5d
H/W Reset	5d	5d	5d	5d

Flow Chart



6.3.9. PWCTR2 (C1H): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1H)
1st Parameter	1	↑	1		0	0	0	0	0	BT2	BT1	BT0	07h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the AVDD, VCL, VGH and VGL supply power level

BT[2:0]		AVDD		VCL		VGH		VGL	
000	0	2xVDDI	4.75	-1xVDDI	-2.45	4*VDDI	9.80	-3*VDDI	-7.35
001	1	2xVDDI	4.75	-1xVDDI	-2.45	4*VDDI	9.80	-4*VDDI	-9.80
010	2	2xVDDI	4.75	-1xVDDI	-2.45	5*VDDI	12.25	-3*VDDI	-7.35
011	3	2xVDDI	4.75	-1xVDDI	-2.45	5*VDDI	12.25	-4*VDDI	-9.80
100	4	2xVDDI	4.75	-1xVDDI	-2.45	5*VDDI	12.25	-5*VDDI	-12.25
101	5	2xVDDI	4.75	-1xVDDI	-2.45	6*VDDI	14.70	-3*VDDI	-7.35
110	6	2xVDDI	4.75	-1xVDDI	-2.45	6*VDDI	14.70	-4*VDDI	-9.80
111	**7**	**2xVDDI**	**4.75**	**-1xVDDI**	**-2.45**	**6*VDDI**	**14.70**	**-5*VDDI**	**-12.25**

Note: When VCI1=2.5V, Set-up cycle 1 effective=95%, Set-up cycle 2 effective=98%,

Restriction

-If this register not using the register need be reserved.

-The deviation value of VGH/ VGL between with Measurement and Specification: **Max: VGH-VGL<=1V**

-**VGH-VGL** <= 25V

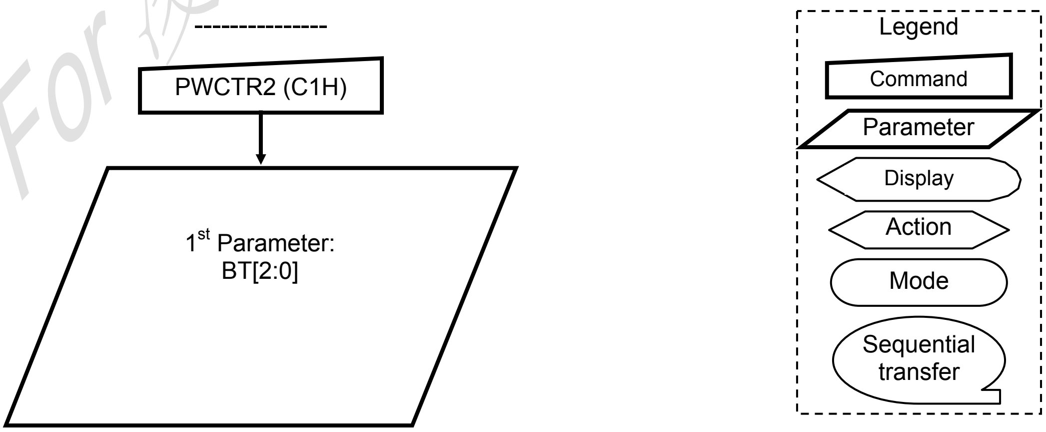
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	BT[2:0]
Power On Sequence	7d
S/W Reset	7d
H/W Reset	7d

Flow Chart



6.3.10. PWCTR3 (C2H): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2H)
1st Parameter	1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0	
2nd Parameter	1	↑	1	-	0	0	0	0	0	DCA2	DCA1	DCA0	01h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the amount of current in Operational amplifier in normal mode/full colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	**4**	**Medium High**
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Normal mode/ full colors.

DC[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 1
001	**1**	**BCLK / 1**	**BCLK / 2**
010	2	BCLK / 1	BCLK / 4
011	3	BCLK / 2	BCLK / 2
100	4	BCLK / 2	BCLK / 4
101	5	BCLK / 4	BCLK / 4
110	6	BCLK / 4	BCLK / 8
111	7	BCLK / 4	BCLK / 16

Note: BCLK is Clock frequency for Booster circuit

Restriction

-If some parameters of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176x220 memory base (GM1, GM0 = “00”)

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	4d	1d
S/W Reset	No Change	No Change
H/W Reset	4d	1d

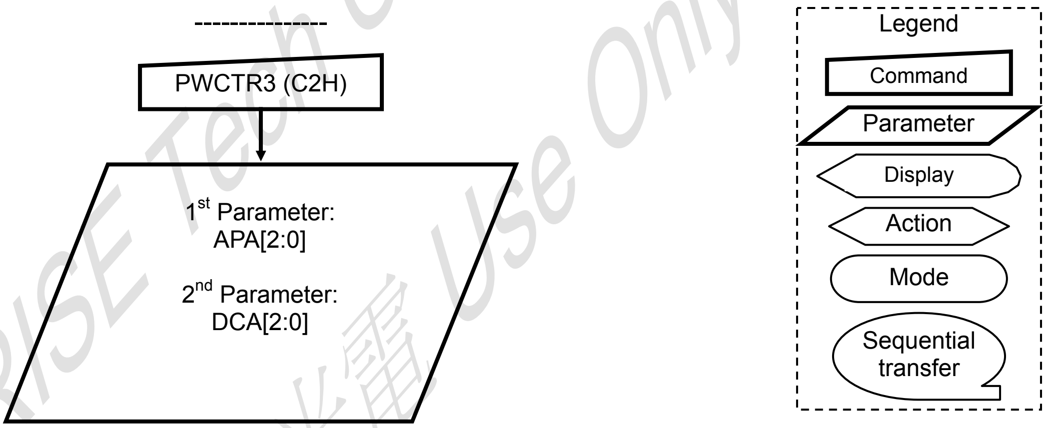
2. 176x176 memory base (GM1, GM0 = “01”)

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	4d	1d
S/W Reset	No Change	No Change
H/W Reset	4d	1d

3. 176x132 memory base (GM1, GM0 = “11”)

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	3d	1d
S/W Reset	No Change	No Change
H/W Reset	3d	1d

Flow Chart



6.3.11. PWCTR4 (C3H): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3H)
1st Parameter	1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0	
2nd Parameter	1	↑	1	-	0	0	0	0	0	DCB2	DCB1	DCB0	04h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the amount of current in Operational amplifier in Idle mode/ 8-colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	**2**	**Medium Low**
011	3	Medium
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Idle mode/ 8-colors.

DC[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 1
001	1	BCLK / 1	BCLK / 2
010	2	BCLK / 1	BCLK / 4
011	3	BCLK / 2	BCLK / 2
100	**4**	**BCLK / 2**	**BCLK / 4**
101	5	BCLK / 4	BCLK / 4
110	6	BCLK / 4	BCLK / 8
111	7	BCLK / 4	BCLK / 16

Note: BCLK is Clock frequency for Booster circuit

Restriction

-If some parameters of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176x220 memory base (GM1, GM0 = “00”)

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	2d	4d
S/W Reset	2d	4d
H/W Reset	2d	4d

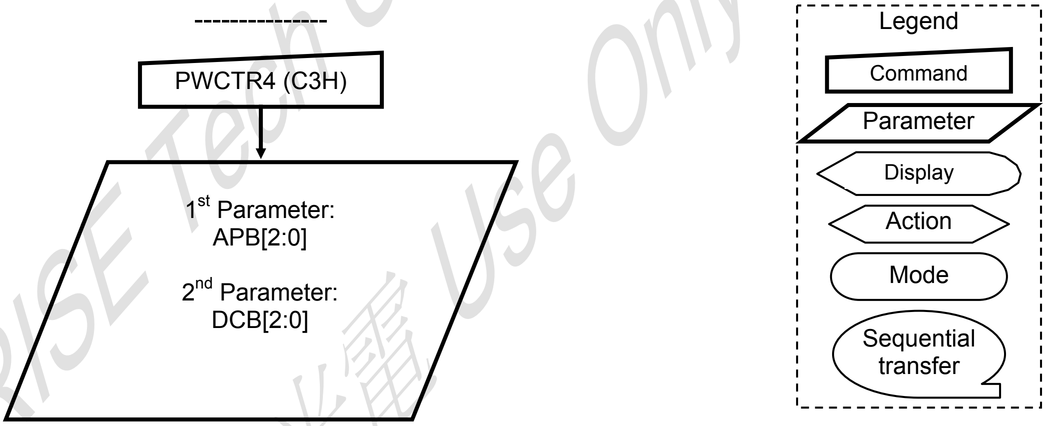
2. 176x176 memory base (GM1, GM0 = “01”)

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	2d	4d
S/W Reset	2d	4d
H/W Reset	2d	4d

3. 176x132 memory base (GM1, GM0 = “11”)

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	2d	4d
S/W Reset	2d	4d
H/W Reset	2d	4d

Flow Chart



6.3.12. PWCTR5 (C4H): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4H)
1st Parameter	1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0	03h
2nd Parameter	1	↑	1	-	0	0	0	0	0	DCC2	DCC1	DCC0	02h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the amount of current in Operational amplifier in Partial mode/ full-colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	**3**	**Medium**
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Partial mode/ full-colors.

DC[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 1
001	1	BCLK / 1	BCLK / 2
010	**2**	**BCLK / 1**	**BCLK / 4**
011	3	BCLK / 2	BCLK / 2
100	4	BCLK / 2	BCLK / 4
101	5	BCLK / 4	BCLK / 4
110	6	BCLK / 4	BCLK / 8
111	7	BCLK / 4	BCLK / 16

Note: BCLK is Clock frequency for Booster circuit

Restriction

-If some parameters of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176x220 memory base (GM1, GM0 = "00")

Status	Default Value	
	APC[2:0]	DCC[2:0]
Power On Sequence	4d	2d
S/W Reset	4d	2d
H/W Reset	4d	2d

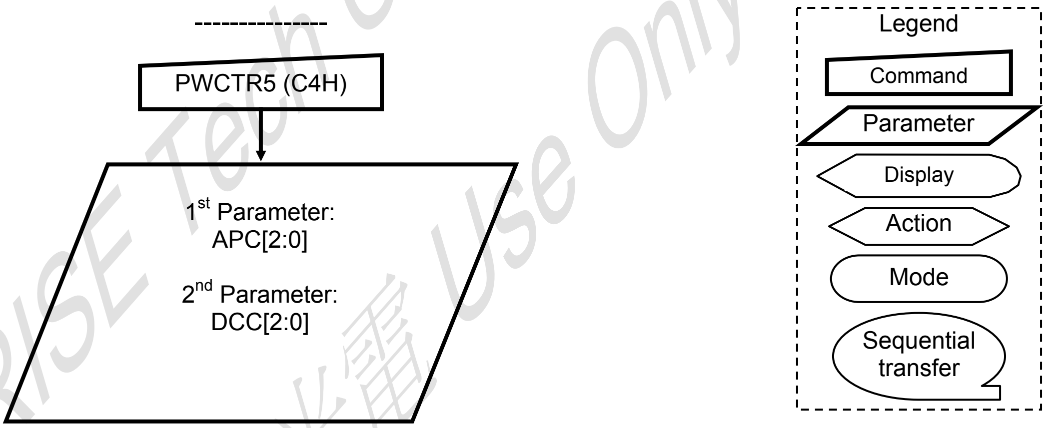
2. 176x176 memory base (GM1, GM0 = "01")

Status	Default Value	
	APC[2:0]	DCC[2:0]
Power On Sequence	4d	2d
S/W Reset	4d	2d
H/W Reset	4d	2d

3. 176x132 memory base (GM1, GM0 = "11")

Status	Default Value	
	APC[2:0]	DCC[2:0]
Power On Sequence	3d	2d
S/W Reset	3d	2d
H/W Reset	3d	2d

Flow Chart



6.3.13. VMCTR1 (C5H): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st Parameter	1	↑	1	-	nVM *	VMH6	VMH5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set **VCOMH** Voltage

VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH
0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525
0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550
0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575
0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600
0000100	4	2.600	0011111	31	3.275	0111010	58	3.950	1010101	85	4.625
0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650
0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675
0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700
0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725
0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750
0001010	10	2.750	0100101	37	3.425	1000000	64	4.100	1011011	91	4.775
0001011	11	2.775	0100110	38	3.450	1000001	65	4.125	1011100	92	4.800
0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825
0001101	13	2.825	**0101000**	**40**	**3.500**	1000011	67	4.175	1011110	94	4.850
0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875
0001111	15	2.875	0101010	42	3.550	1000101	69	4.225	1100000	96	4.900
0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925
0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950
0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975
0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000
0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101	Not Permitted
0010101	21	3.025	0110000	48	3.700	1001011	75	4.375		|	
0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	1111111	127	
0010111	23	3.075	0110010	50	3.750	1001101	77	4.425			
0011000	24	3.100	0110011	51	3.775	1001110	78	4.450			
0011001	25	3.125	0110100	52	3.800	1001111	79	4.475			
0011010	**26**	**3.150**	0110101	53	3.825	1010000	80	4.500			

-Select the VCOMH value

nVM *	VCOMH value
0	**VCOMH value is from NV memory**
1	VCOMH value is from the VCOMH[6:0] setting

-The nVM need be used in 1st parameter of VMCTR1 (C5h)
- When nVM=0, the value of VMH[6:0] is from NV memory. So it must program the NV memory first.
- When nVM=1, the vaule of VMH[6:0] is from $C5 register. It can fine-tune the display performance to the best quality by setting this register, and program this optium value to NV memory.

Restriction

-If this register not using the register need be reserved.

-The deviation value of VCOMH between with Measurement and Specification: **Max <=25mV**

-The deviation value of VCOMAC between with Measurement and Specification: **Max <=50mV**

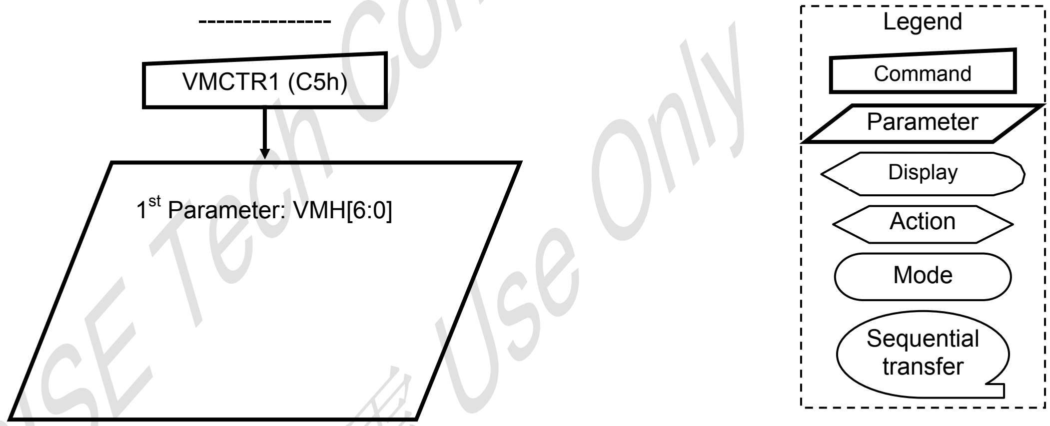
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	nVM	LCM = ‘11’	LCM = ‘01’
		VMH[6:0]	VMH[6:0]
Power On Sequence	0d	40d	26d
S/W Reset	0d	40d	26d
H/W Reset	0d	40d	26d

Flow Chart



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6.3.14. VMCTR2 (C6H): VCOM Control 2

C6H	VMCTR2 (VCOM Control 2)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR2	0	↑	1	-	1	1	0	0	0	1	1	0	(C6H)
1st Parameter	1	↑	1	-	0	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set **VCOMAC** Voltage

VMA[5:0]		VCOMAC	VMA[5:0]		VCOMAC	VMA[5:0]		VCOMAC
000000	0	4.000	010000	16	4.800	100000	32	5.600
000001	1	4.050	010001	17	4.850	100001	33	5.650
000010	2	4.100	010010	18	4.900	100010	34	5.700
000011	3	4.150	010011	19	4.950	100011	35	5.750
000100	4	4.200	010100	20	5.000	100100	36	5.800
000101	5	4.250	**010101**	**21**	**5.050**	100101	37	5.850
000110	6	4.300	010110	22	5.100	100110	38	5.900
000111	7	4.350	010111	23	5.150	100111	39	5.950
001000	8	4.400	011000	24	5.200	101000	40	6.000
001001	9	4.450	011001	25	5.250	101001	41	Not Permitted
001010	10	4.500	011010	26	5.300		|	
001011	11	4.550	011011	27	5.350	111111	63	
001100	12	4.600	011100	28	5.400			
001101	13	4.650	011101	29	5.450			
001110	14	4.700	011110	30	5.500			
001111	15	4.750	011111	31	5.550			

Restriction

-If this register not use the register need be reserved.

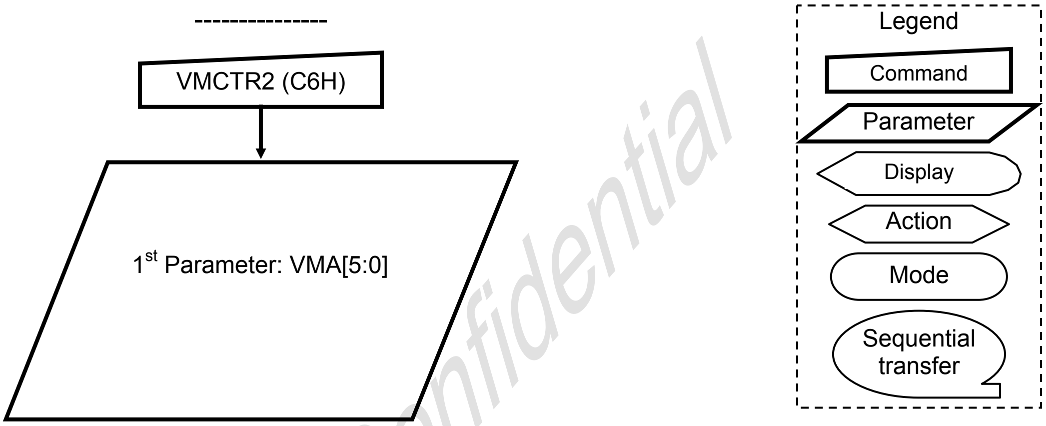
-The deviation value of VCOMAC between with Measurement and Specification: **Max <=50mV**

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	LCM = '01' TM LC Type	LCM = '11' ECB LC type
	VMA[5:0]	VMA[5:0]
Power On Sequence	21d	21d
S/W Reset	21d	21d
H/W Reset	21d	21d

Flow Chart	 --------------- VMCTR2 (C6H) 1st Parameter: VMA[5:0] Legend Command Parameter Display Action Mode Sequential transfer

6.3.15. RDVMOF (C8H): Read the VCOM Offset Value NV memory

C8H	RDVMOF (Read the VCOM Offset Value NV memory)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDVMOF	0	↑	1	-	1	1	0	0	1	0	0	0	(C8H)
1st Parameter	0	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	nVM	RVMF6	RVMF5	RVMF4	RVMF3	RVMF2	RVMF1	RVMF0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Read the VCOM offset value from NV memory

-The 1st parameter is dummy data.

-The 2nd parameter is VMF[6:0] value from NV memory or default value.

Restriction

-If this register not use the register need be reserved.

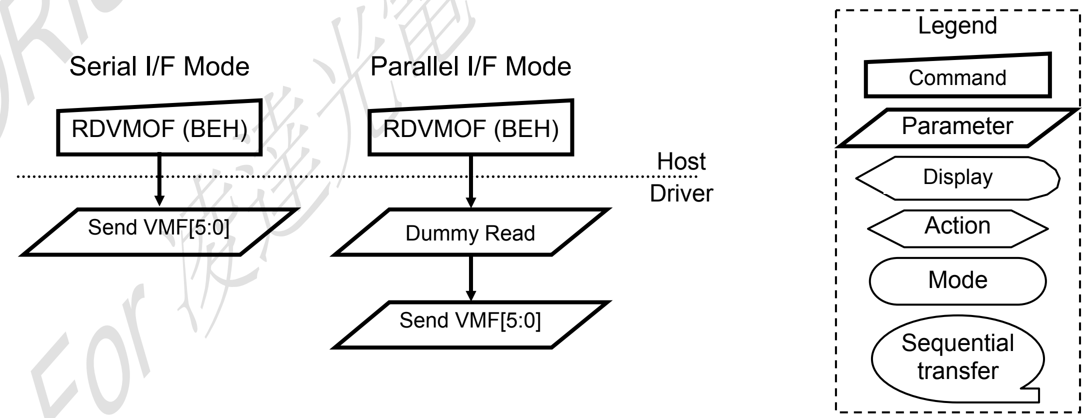
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value-
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



6.3.16. WRID2 (D1h): Write ID2 Value

D0H	WRID2 (Write ID2 Value)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
1st Parameter	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description	-Write 7-bits data of LCD module version to save it to NV memory. -The 1st parameter ID2[6:0] is LCD Module version ID.
Restriction	
Register Availability	see table below
Default	see table below
Flow Chart	see chart below

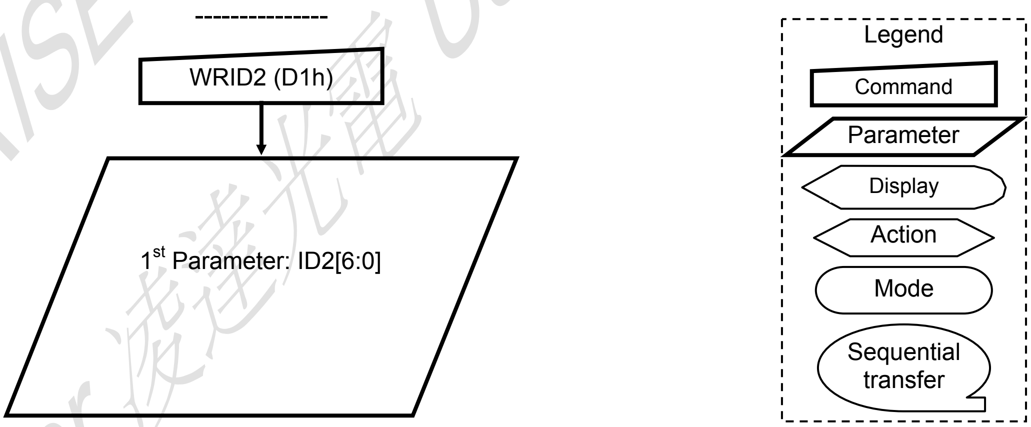
Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

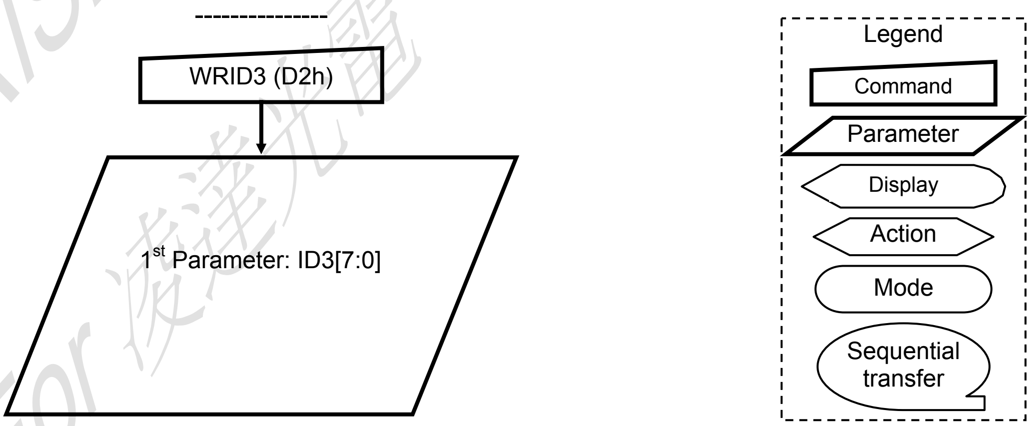
Flow Chart:



6.3.17. WRID3 (D2h): Write ID3 Value

D0H	WRID3 (Write ID3 Value)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
1st Parameter	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>-Write 8-bits data of project code module to save it to NV memory.
-The 1st parameter ID3[7:0] is product project ID.</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

6.3.18. RDID4 (D3h): Read the ID4 value

D4H	RDID4 (Read the ID4 value)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID4	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	-
3rd Parameter	1	1	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	-
4th Parameter	1	1	↑	-	ID437	ID436	ID435	ID434	ID433	ID432	ID431	ID430	-
5th Parameter	1	1	↑	-	ID447	ID446	ID445	ID444	ID443	ID442	ID441	ID440	-

NOTE: "-" Don't care

Description

-Read the Driver IC information from mask value.
-The 1st parameter is dummy data.
-The 2nd parameter ID41[7:0] is Driver IC ID code.
  -ID41[7:0] is 06H.
-The 3rd parameter ID42[7:0] is Driver IC Part number ID. It is 16H.
-The 4th & 5th parameter ID43[7:0] & ID44[7:0] are Driver IC version ID.

Restriction

-

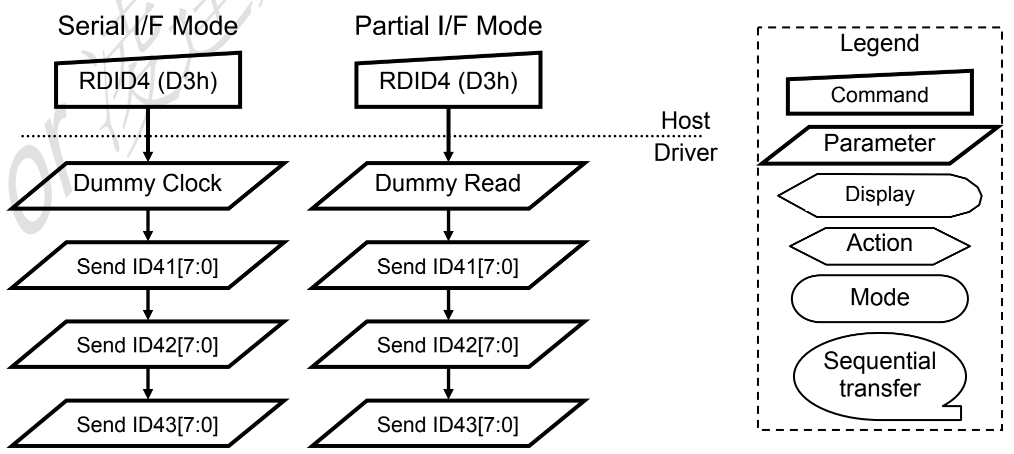
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value-			
	ID41[7:0]	ID42[7:0]	ID43[7:0]	ID44[7:0]
Power On Sequence	06H	14H	00H	00H
S/W Reset	06H	14H	00H	00H
H/W Reset	06H	14H	00H	00H

Flow Chart



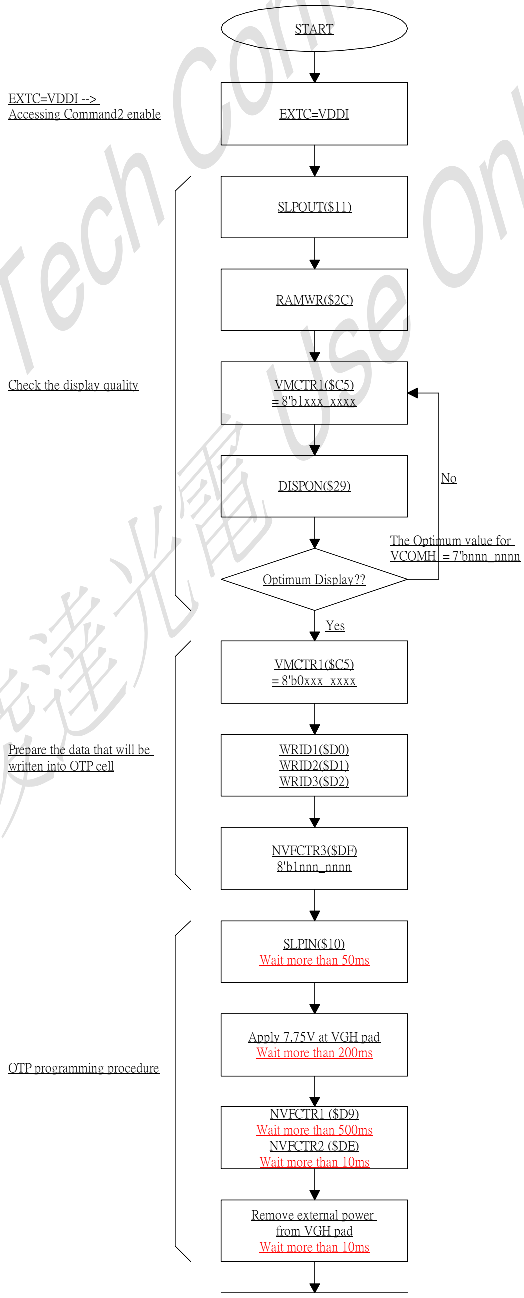
6.3.19. NVFCTR1 (D9h): NV Memory Function Controller 1

D9H	NVFCTR1 (NV Memory Function Controller 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR1	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)
1st Parameter	1	↑	1	-	WVMH 7	WVMH 6	WVMH 5	WVMH 4	WVMH 3	WVMH 2	WVMH 1	WVMH 0	-

NOTE: "-" Don't care1

Description

- Write WVMH[6:0] for VCOMH voltage to $D9 when the value is considered as the optimum for display quality.
- The endurence for SPFD54126B NV memory is 4 times for VCOMH, ID1, ID2 and ID3.



Restriction	The endurence of WVMH, ID1, ID2, and ID3 is 4 times.

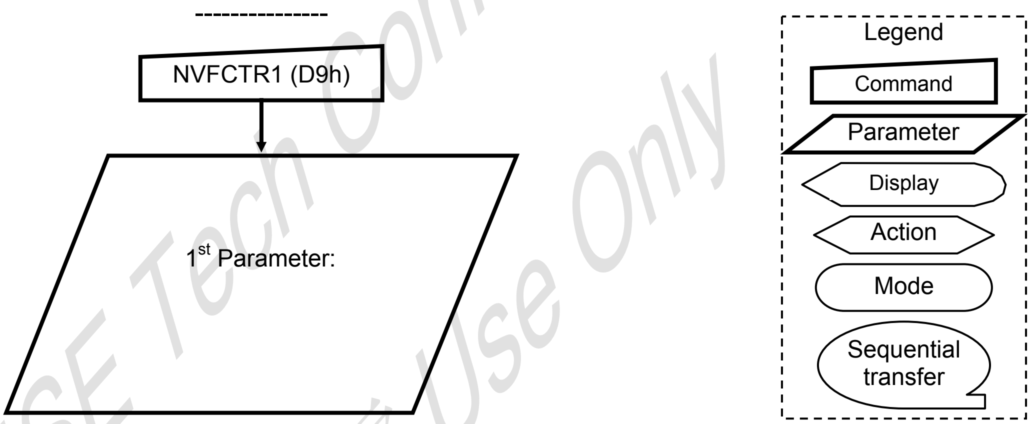
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

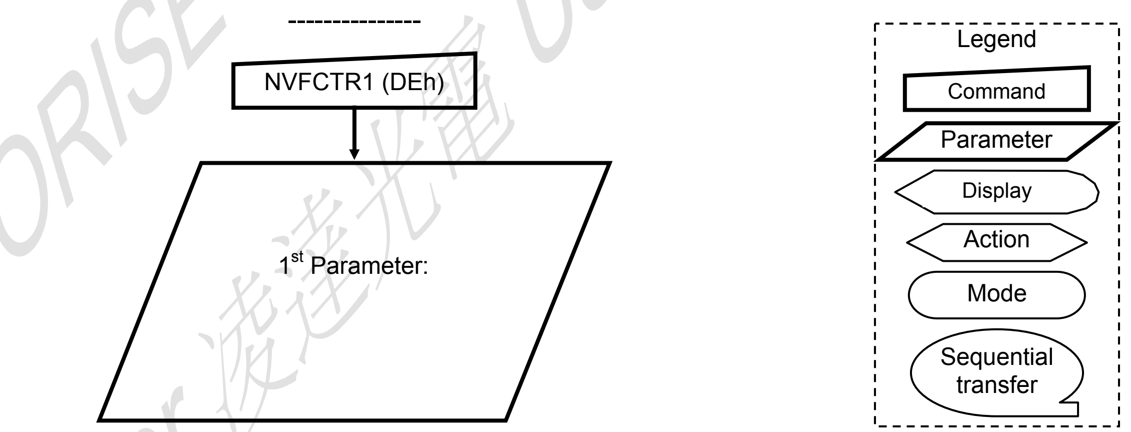
Flow Chart



6.3.20. NVFCTR2 (DEh): NV Memory Function Controller 2

DEH	NVFCTR2 (NV Memory Function Controller 2)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR2	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)
1st Parameter	1	↑	1	-	1								-

NOTE: "-" Don't care

Description	**- Please refer to $D9 for details.**
Restriction	
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Not Fixed</td></tr><tr><td>S/W Reset</td><td>Not Fixed</td></tr><tr><td>H/W Reset</td><td>Not Fixed</td></tr></table>
Flow Chart	

6.3.21. NVFCTR3 (DFh): NV Memory Function Controller 3

DEH	NVFCTR3 (NV Memory Function Controller 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR3	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
1st Parameter	1	↑	1	-	1								-

NOTE: "-" Don't care

Description	**- Please refer to $D9 for details.**
Restriction	

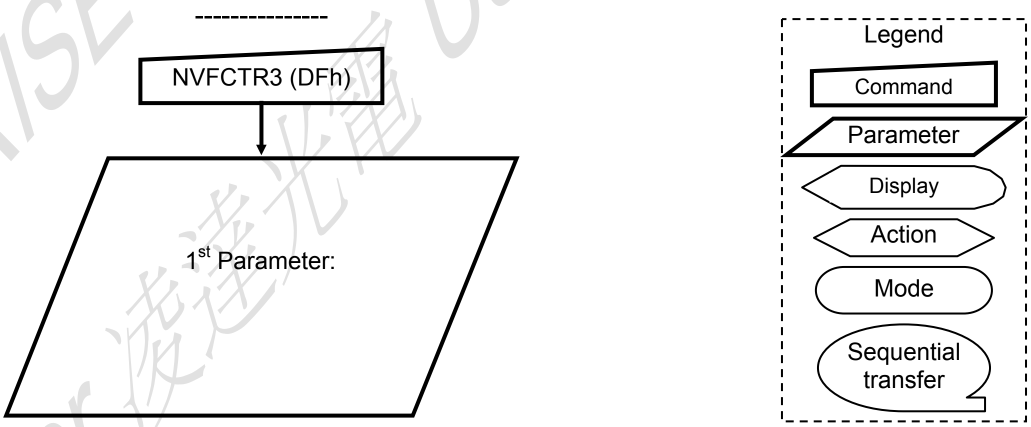
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



6.3.22. GMCTRP1 (E0H): Gamma ('+'polarity for Red color) Correction Characteristics Setting

E0H	GMCTRP1 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st Parameter	1	↑	1	-	-	-	-	R_PVR1 V0[4]	R_PVR1 V0[3]	R_PVR1 V0[2]	R_PVR1 V0[1]	R_PVR1 V0[0]	
2nd Parameter	1	↑	1	-	-	-	R_PVR1 V1[5]	R_PVR1 V1[4]	R_PVR1 V1[3]	R_PVR1 V1[2]	R_PVR1 V1[1]	R_PVR1 V1[0]	
3rd Parameter	1	↑	1	-	-	-	R_PVR1 V2[5]	R_PVR1 V2[4]	R_PVR1 V2[3]	R_PVR1 V2[2]	R_PVR1 V2[1]	R_PVR1 V2[0]	
4th Parameter	1	↑	1	-	-	-	R_PVR1 V61[5]	R_PVR1 V61[4]	R_PVR1 V61[3]	R_PVR1 V61[2]	R_PVR1 V61[1]	R_PVR1 V61[0]	
5th Parameter	1	↑	1	-	-	-	R_PVR1 V62[5]	R_PVR1 V62[4]	R_PVR1 V62[3]	R_PVR1 V62[2]	R_PVR1 V62[1]	R_PVR1 V62[0]	
6th Parameter	1	↑	1	-	-	-	-	R_PVR1 V63[4]	R_PVR1 V63[3]	R_PVR1 V63[2]	R_PVR1 V63[1]	R_PVR1 V63[0]	
7th Parameter	1	↑	1	-	-	-	-	R_PVR2 V13[4]	R_PVR2 V13[3]	R_PVR2 V13[2]	R_PVR2 V13[1]	R_PVR2 V13[0]	
8th Parameter	1	↑	1	-	-	-	-	R_PVR2 V50[4]	R_PVR2 V50[3]	R_PVR2 V50[2]	R_PVR2 V50[1]	R_PVR2 V50[0]	
9th Parameter	1	↑	1	-	-	-	-	-	R_PVR3 V4[3]	R_PVR3 V4[2]	R_PVR3 V4[1]	R_PVR3 V4[0]	
10th Parameter	1	↑	1	-	-	-	-	-	R_PVR3 V8[3]	R_PVR3 V8[2]	R_PVR3 V8[1]	R_PVR3 V8[0]	
11th Parameter	1	↑	1	-	-	-	-	-	R_PVR3 V20[3]	R_PVR3 V20[2]	R_PVR3 V20[1]	R_PVR3 V20[0]	
12th Parameter	1	↑	1	-	-	-	-	-	R_PVR3 V27[3]	R_PVR3 V27[2]	R_PVR3 V27[1]	R_PVR3 V27[0]	
13th Parameter	1	↑	1	-	-	-	-	-	R_PVR3 V36[3]	R_PVR3 V36[2]	R_PVR3 V36[1]	R_PVR3 V36[0]	
14th Parameter	1	↑	1	-	-	-	-	-	R_PVR3 V43[3]	R_PVR3 V43[2]	R_PVR3 V43[1]	R_PVR3 V43[0]	
15th Parameter	1	↑	1	-	-	-	-	-	R_PVR3 V55[3]	R_PVR3 V55[2]	R_PVR3 V55[1]	R_PVR3 V55[0]	
16th Parameter	1	↑	1	-	-	-	-	-	R_PVR3 V59[3]	R_PVR3 V59[2]	R_PVR3 V59[1]	R_PVR3 V59[0]	

NOTE: "-" Don't care

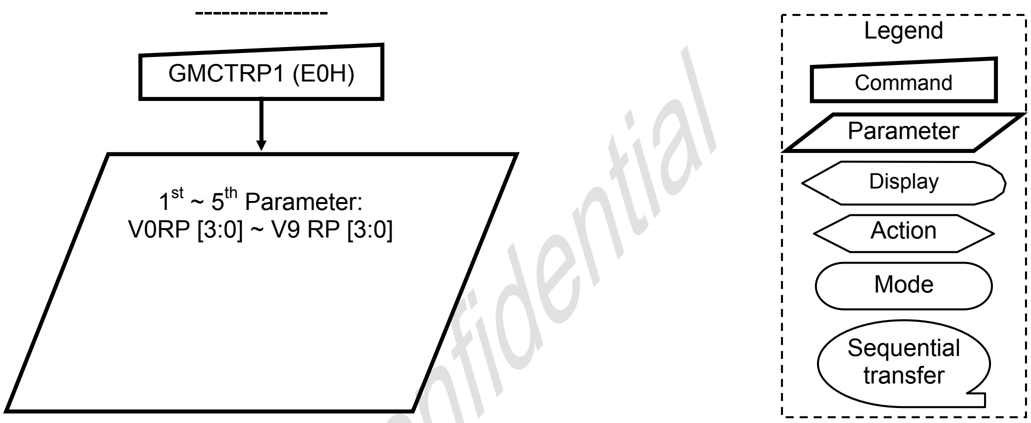
Description	-When turn ON the separate RGB gamma function the command is used for **R gamma** ('+'polarity) of GC0 correction characteristics setting -When turn OFF the separate RGB gamma function the command is used for gamma ('+' polarity) correction characteristics setting
Restriction	

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	----
S/W Reset	----
H/W Reset	----

Flow Chart	 ---------------- GMCTRP1 (E0H) 1st ~ 5th Parameter: V0RP [3:0] ~ V9 RP [3:0] Legend Command Parameter Display Action Mode Sequential transfer

6.3.23. GMCTRN1 (E1H): Gamma ('-'polarity for Red color) Correction Characteristics Setting

E1H	GMCTRP1 (Gamma '+'polarity Correction Characteristics Setting)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E1h)
1st Parameter	1	↑	1	-	-	-	-	R_NVR1 V0[4]	R_NVR1 V0[3]	R_NVR1 V0[2]	R_NVR1 V0[1]	R_NVR1 V0[0]	
2nd Parameter	1	↑	1	-	-	-	R_NVR1 V1[5]	R_NVR1 V1[4]	R_NVR1 V1[3]	R_NVR1 V1[2]	R_NVR1 V1[1]	R_NVR1 V1[0]	
3rd Parameter	1	↑	1	-	-	-	R_NVR1 V2[5]	R_NVR1 V2[4]	R_NVR1 V2[3]	R_NVR1 V2[2]	R_NVR1 V2[1]	R_NVR1 V2[0]	
4th Parameter	1	↑	1	-	-	-	R_NVR1 V61[5]	R_NVR1 V61[4]	R_NVR1 V61[3]	R_NVR1 V61[2]	R_NVR1 V61[1]	R_NVR1 V61[0]	
5th Parameter	1	↑	1	-	-	-	R_NVR1 V62[5]	R_NVR1 V62[4]	R_NVR1 V62[3]	R_NVR1 V62[2]	R_NVR1 V62[1]	R_NVR1 V62[0]	
6th Parameter	1	↑	1	-	-	-	-	R_NVR1 V63[4]	R_NVR1 V63[3]	R_NVR1 V63[2]	R_NVR1 V63[1]	R_NVR1 V63[0]	
7th Parameter	1	↑	1	-	-	-	-	R_NVR2 V13[4]	R_NVR2 V13[3]	R_NVR2 V13[2]	R_NVR2 V13[1]	R_NVR2 V13[0]	
8th Parameter	1	↑	1	-	-	-	-	R_NVR2 V50[4]	R_NVR2 V50[3]	R_NVR2 V50[2]	R_NVR2 V50[1]	R_NVR2 V50[0]	
9th Parameter	1	↑	1	-	-	-	-	-	R_NVR3 V4[3]	R_NVR3 V4[2]	R_NVR3 V4[1]	R_NVR3 V4[0]	
10th Parameter	1	↑	1	-	-	-	-	-	R_NVR3 V8[3]	R_NVR3 V8[2]	R_NVR3 V8[1]	R_NVR3 V8[0]	
11th Parameter	1	↑	1	-	-	-	-	-	R_NVR3 V20[3]	R_NVR3 V20[2]	R_NVR3 V20[1]	R_NVR3 V20[0]	
12th Parameter	1	↑	1	-	-	-	-	-	R_NVR3 V27[3]	R_NVR3 V27[2]	R_NVR3 V27[1]	R_NVR3 V27[0]	
13th Parameter	1	↑	1	-	-	-	-	-	R_NVR3 V36[3]	R_NVR3 V36[2]	R_NVR3 V36[1]	R_NVR3 V36[0]	
14th Parameter	1	↑	1	-	-	-	-	-	R_NVR3 V43[3]	R_NVR3 V43[2]	R_NVR3 V43[1]	R_NVR3 V43[0]	
15th Parameter	1	↑	1	-	-	-	-	-	R_NVR3 V55[3]	R_NVR3 V55[2]	R_NVR3 V55[1]	R_NVR3 V55[0]	
16th Parameter	1	↑	1	-	-	-	-	-	R_NVR3 V59[3]	R_NVR3 V59[2]	R_NVR3 V59[1]	R_NVR3 V59[0]	

NOTE: "-" Don't care

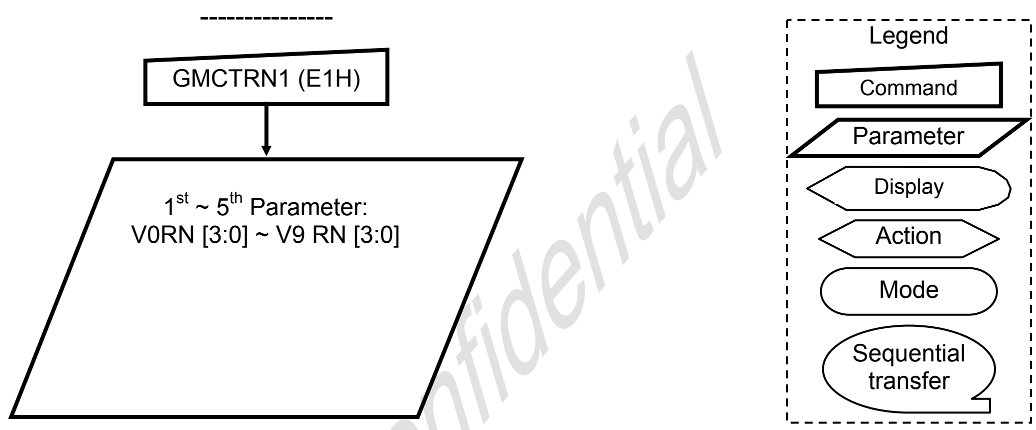
Description	-When turn ON the separate RGB gamma function the command is used for **R gamma** ('-' polarity) of GC0 correction characteristics setting -When turn OFF the separate RGB gamma function the command is used for gamma ('-' polarity) correction characteristics setting
Restriction	
Register Availability	see table below
Default	see table below

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	----
S/W Reset	----
H/W Reset	----

Flow Chart	

GMCTRN1 (E1H)
1st ~ 5th Parameter:
V0RN [3:0] ~ V9 RN [3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.3.24. GMCTRP2 (E2H): Gamma ('+'polarity) for Green color Correction Characteristics Setting

E2H	GMCTRP1 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E2h)
1st Parameter	1	↑	1	-	-	-	-	G_PVR1 V0[4]	G_PVR1 V0[3]	G_PVR1 V0[2]	G_PVR1 V0[1]	G_PVR1 V0[0]	
2nd Parameter	1	↑	1	-	-	-	G_PVR1 V1[5]	G_PVR1 V1[4]	G_PVR1 V1[3]	G_PVR1 V1[2]	G_PVR1 V1[1]	G_PVR1 V1[0]	
3rd Parameter	1	↑	1	-	-	-	G_PVR1 V2[5]	G_PVR1 V2[4]	G_PVR1 V2[3]	G_PVR1 V2[2]	G_PVR1 V2[1]	G_PVR1 V2[0]	
4th Parameter	1	↑	1	-	-	-	G_PVR1 V61[5]	G_PVR1 V61[4]	G_PVR1 V61[3]	G_PVR1 V61[2]	G_PVR1 V61[1]	G_PVR1 V61[0]	
5th Parameter	1	↑	1	-	-	-	G_PVR1 V62[5]	G_PVR1 V62[4]	G_PVR1 V62[3]	G_PVR1 V62[2]	G_PVR1 V62[1]	G_PVR1 V62[0]	
6th Parameter	1	↑	1	-	-	-	-	G_PVR1 V63[4]	G_PVR1 V63[3]	G_PVR1 V63[2]	G_PVR1 V63[1]	G_PVR1 V63[0]	
7th Parameter	1	↑	1	-	-	-	-	G_PVR2 V13[4]	G_PVR2 V13[3]	G_PVR2 V13[2]	G_PVR2 V13[1]	G_PVR2 V13[0]	
8th Parameter	1	↑	1	-	-	-	-	G_PVR2 V50[4]	G_PVR2 V50[3]	G_PVR2 V50[2]	G_PVR2 V50[1]	G_PVR2 V50[0]	
9th Parameter	1	↑	1	-	-	-	-	-	G_PVR3 V4[3]	G_PVR3 V4[2]	G_PVR3 V4[1]	G_PVR3 V4[0]	
10th Parameter	1	↑	1	-	-	-	-	-	G_PVR3 V8[3]	G_PVR3 V8[2]	G_PVR3 V8[1]	G_PVR3 V8[0]	
11th Parameter	1	↑	1	-	-	-	-	-	G_PVR3 V20[3]	G_PVR3 V20[2]	G_PVR3 V20[1]	G_PVR3 V20[0]	
12th Parameter	1	↑	1	-	-	-	-	-	G_PVR3 V27[3]	G_PVR3 V27[2]	G_PVR3 V27[1]	G_PVR3 V27[0]	
13th Parameter	1	↑	1	-	-	-	-	-	G_PVR3 V36[3]	G_PVR3 V36[2]	G_PVR3 V36[1]	G_PVR3 V36[0]	
14th Parameter	1	↑	1	-	-	-	-	-	G_PVR3 V43[3]	G_PVR3 V43[2]	G_PVR3 V43[1]	G_PVR3 V43[0]	
15th Parameter	1	↑	1	-	-	-	-	-	G_PVR3 V55[3]	G_PVR3 V55[2]	G_PVR3 V55[1]	G_PVR3 V55[0]	
16th Parameter	1	↑	1	-	-	-	-	-	G_PVR3 V59[3]	G_PVR3 V59[2]	G_PVR3 V59[1]	G_PVR3 V59[0]	

NOTE: "-" Don't care

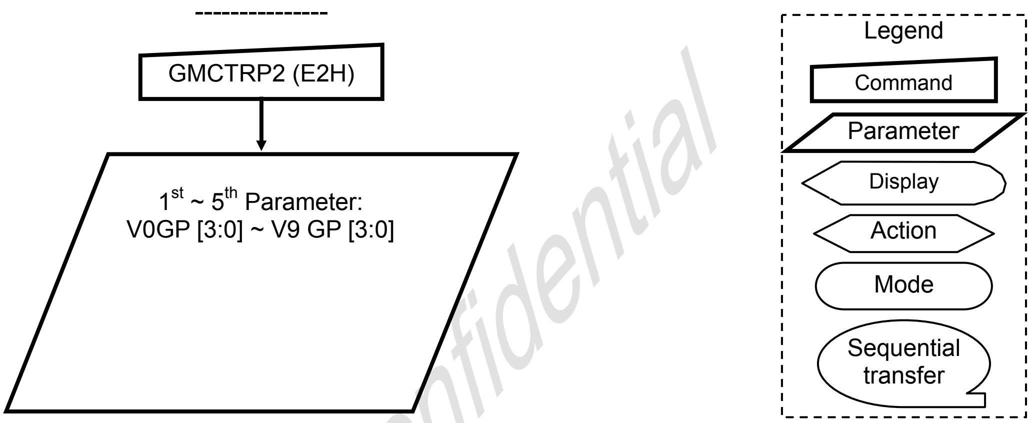
Description	-When turn ON the separate RGB gamma function the command is only used for **G gamma** ('+'polarity) of GC0 correction characteristics setting -When turn OFF the separate RGB gamma function the command is not used.
Restriction	
Register Availability	(see table below)
Default	(see table below)

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	----
S/W Reset	----
H/W Reset	----

Flow Chart	---------------- GMCTRP2 (E2H) 1st ~ 5th Parameter: V0GP [3:0] ~ V9 GP [3:0] Legend Command Parameter Display Action Mode Sequential transfer

6.3.25. GMCTRN2 (E3H): Gamma ('-'polarity) for Green color Correction Characteristics Setting

E3H	GMCTRP1 (Gamma '+'polarity Correction Characteristics Setting)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E3h)
1st Parameter	1	↑	1	-	-	-	-	G_NVR1 V0[4]	G_NVR1 V0[3]	G_NVR1 V0[2]	G_NVR1 V0[1]	G_NVR1 V0[0]	
2nd Parameter	1	↑	1	-	-	-	G_NVR1 V1[5]	G_NVR1 V1[4]	G_NVR1 V1[3]	G_NVR1 V1[2]	G_NVR1 V1[1]	G_NVR1 V1[0]	
3rd Parameter	1	↑	1	-	-	-	G_NVR1 V2[5]	G_NVR1 V2[4]	G_NVR1 V2[3]	G_NVR1 V2[2]	G_NVR1 V2[1]	G_NVR1 V2[0]	
4th Parameter	1	↑	1	-	-	-	G_NVR1 V61[5]	G_NVR1 V61[4]	G_NVR1 V61[3]	G_NVR1 V61[2]	G_NVR1 V61[1]	G_NVR1 V61[0]	
5th Parameter	1	↑	1	-	-	-	G_NVR1 V62[5]	G_NVR1 V62[4]	G_NVR1 V62[3]	G_NVR1 V62[2]	G_NVR1 V62[1]	G_NVR1 V62[0]	
6th Parameter	1	↑	1	-	-	-	-	G_NVR1 V63[4]	G_NVR1 V63[3]	G_NVR1 V63[2]	G_NVR1 V63[1]	G_NVR1 V63[0]	
7th Parameter	1	↑	1	-	-	-	-	G_NVR2 V13[4]	G_NVR2 V13[3]	G_NVR2 V13[2]	G_NVR2 V13[1]	G_NVR2 V13[0]	
8th Parameter	1	↑	1	-	-	-	-	G_NVR2 V50[4]	G_NVR2 V50[3]	G_NVR2 V50[2]	G_NVR2 V50[1]	G_NVR2 V50[0]	
9th Parameter	1	↑	1	-	-	-	-	-	G_NVR3 V4[3]	G_NVR3 V4[2]	G_NVR3 V4[1]	G_NVR3 V4[0]	
10th Parameter	1	↑	1	-	-	-	-	-	G_NVR3 V8[3]	G_NVR3 V8[2]	G_NVR3 V8[1]	G_NVR3 V8[0]	
11th Parameter	1	↑	1	-	-	-	-	-	G_NVR3 V20[3]	G_NVR3 V20[2]	G_NVR3 V20[1]	G_NVR3 V20[0]	
12th Parameter	1	↑	1	-	-	-	-	-	G_NVR3 V27[3]	G_NVR3 V27[2]	G_NVR3 V27[1]	G_NVR3 V27[0]	
13th Parameter	1	↑	1	-	-	-	-	-	G_NVR3 V36[3]	G_NVR3 V36[2]	G_NVR3 V36[1]	G_NVR3 V36[0]	
14th Parameter	1	↑	1	-	-	-	-	-	G_NVR3 V43[3]	G_NVR3 V43[2]	G_NVR3 V43[1]	G_NVR3 V43[0]	
15th Parameter	1	↑	1	-	-	-	-	-	G_NVR3 V55[3]	G_NVR3 V55[2]	G_NVR3 V55[1]	G_NVR3 V55[0]	
16th Parameter	1	↑	1	-	-	-	-	-	G_NVR3 V59[3]	G_NVR3 V59[2]	G_NVR3 V59[1]	G_NVR3 V59[0]	

NOTE: "-" Don't care

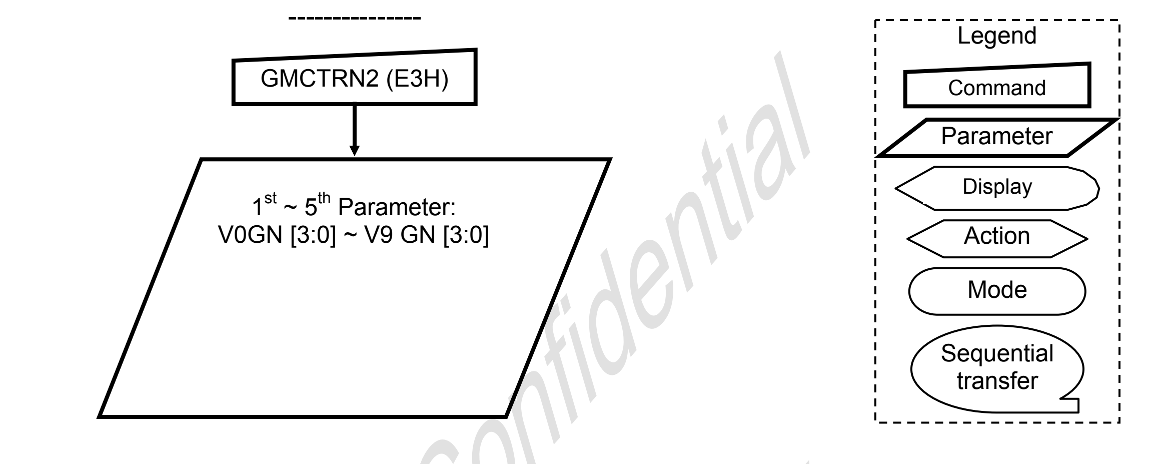
Description	-When turn ON the separate RGB gamma function the command is only used for **G gamma** ('-' polarity) of GC0 correction characteristics setting -When turn OFF the separate RGB gamma function the command is not used.
Restriction	
Register Availability	(see table below)
Default	(see table below)

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	----
S/W Reset	----
H/W Reset	----

Flow Chart	

GMCTRN2 (E3H)
1st ~ 5th Parameter:
V0GN [3:0] ~ V9 GN [3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.3.26. GMCTRP3 (E4H): Gamma ('+'polarity) for Blue color correction Characteristics Setting

E4H	GMCTRP1 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E4h)
1st Parameter	1	↑	1	-	-	-	-	B_PVR1 V0[4]	B_PVR1 V0[3]	B_PVR1 V0[2]	B_PVR1 V0[1]	B_PVR1 V0[0]	
2nd Parameter	1	↑	1	-	-	-	B_PVR1 V1[5]	B_PVR1 V1[4]	B_PVR1 V1[3]	B_PVR1 V1[2]	B_PVR1 V1[1]	B_PVR1 V1[0]	
3rd Parameter	1	↑	1	-	-	-	B_PVR1 V2[5]	B_PVR1 V2[4]	B_PVR1 V2[3]	B_PVR1 V2[2]	B_PVR1 V2[1]	B_PVR1 V2[0]	
4th Parameter	1	↑	1	-	-	-	B_PVR1 V61[5]	B_PVR1 V61[4]	B_PVR1 V61[3]	B_PVR1 V61[2]	B_PVR1 V61[1]	B_PVR1 V61[0]	
5th Parameter	1	↑	1	-	-	-	B_PVR1 V62[5]	B_PVR1 V62[4]	B_PVR1 V62[3]	B_PVR1 V62[2]	B_PVR1 V62[1]	B_PVR1 V62[0]	
6th Parameter	1	↑	1	-	-	-	-	B_PVR1 V63[4]	B_PVR1 V63[3]	B_PVR1 V63[2]	B_PVR1 V63[1]	B_PVR1 V63[0]	
7th Parameter	1	↑	1	-	-	-	-	B_PVR2 V13[4]	B_PVR2 V13[3]	B_PVR2 V13[2]	B_PVR2 V13[1]	B_PVR2 V13[0]	
8th Parameter	1	↑	1	-	-	-	-	B_PVR2 V50[4]	B_PVR2 V50[3]	B_PVR2 V50[2]	B_PVR2 V50[1]	B_PVR2 V50[0]	
9th Parameter	1	↑	1	-	-	-	-	-	B_PVR3 V4[3]	B_PVR3 V4[2]	B_PVR3 V4[1]	B_PVR3 V4[0]	
10th Parameter	1	↑	1	-	-	-	-	-	B_PVR3 V8[3]	B_PVR3 V8[2]	B_PVR3 V8[1]	B_PVR3 V8[0]	
11th Parameter	1	↑	1	-	-	-	-	-	B_PVR3 V20[3]	B_PVR3 V20[2]	B_PVR3 V20[1]	B_PVR3 V20[0]	
12th Parameter	1	↑	1	-	-	-	-	-	B_PVR3 V27[3]	B_PVR3 V27[2]	B_PVR3 V27[1]	B_PVR3 V27[0]	
13th Parameter	1	↑	1	-	-	-	-	-	B_PVR3 V36[3]	B_PVR3 V36[2]	B_PVR3 V36[1]	B_PVR3 V36[0]	
14th Parameter	1	↑	1	-	-	-	-	-	B_PVR3 V43[3]	B_PVR3 V43[2]	B_PVR3 V43[1]	B_PVR3 V43[0]	
15th Parameter	1	↑	1	-	-	-	-	-	B_PVR3 V55[3]	B_PVR3 V55[2]	B_PVR3 V55[1]	B_PVR3 V55[0]	
16th Parameter	1	↑	1	-	-	-	-	-	B_PVR3 V59[3]	B_PVR3 V59[2]	B_PVR3 V59[1]	B_PVR3 V59[0]	

NOTE: "-" Don't care

Description	-When turn ON the separate RGB gamma function the command is only used for **B gamma** ('+'polarity) of GC0 correction characteristics setting -When turn OFF the separate RGB gamma function the command is not used.
Restriction	
Register Availability	see table below
Default	see table below

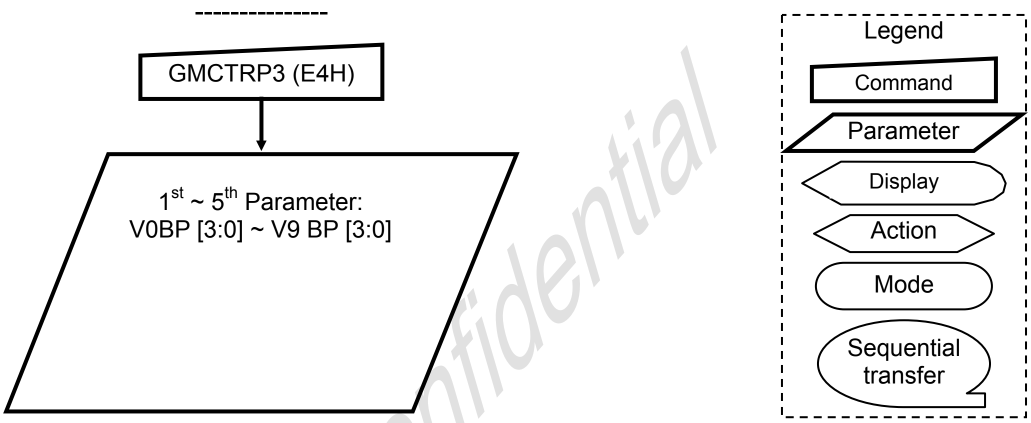
Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	----
S/W Reset	----
H/W Reset	----

Flow Chart



GMCTRP3 (E4H)
1st ~ 5th Parameter:
V0BP [3:0] ~ V9 BP [3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.3.27. GMCTRN3 (E5H): Gamma ('-'polarity) for Blue color Correction Characteristics Setting

E5H	GMCTRP1 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E5h)
1st Parameter	1	↑	1	-	-	-	-	B_NVR1 V0[4]	B_NVR1 V0[3]	B_NVR1 V0[2]	B_NVR1 V0[1]	B_NVR1 V0[0]	
2nd Parameter	1	↑	1	-	-	-	B_NVR1 V1[5]	B_NVR1 V1[4]	B_NVR1 V1[3]	B_NVR1 V1[2]	B_NVR1 V1[1]	B_NVR1 V1[0]	
3rd Parameter	1	↑	1	-	-	-	B_NVR1 V2[5]	B_NVR1 V2[4]	B_NVR1 V2[3]	B_NVR1 V2[2]	B_NVR1 V2[1]	B_NVR1 V2[0]	
4th Parameter	1	↑	1	-	-	-	B_NVR1 V61[5]	B_NVR1 V61[4]	B_NVR1 V61[3]	B_NVR1 V61[2]	B_NVR1 V61[1]	B_NVR1 V61[0]	
5th Parameter	1	↑	1	-	-	-	B_NVR1 V62[5]	B_NVR1 V62[4]	B_NVR1 V62[3]	B_NVR1 V62[2]	B_NVR1 V62[1]	B_NVR1 V62[0]	
6th Parameter	1	↑	1	-	-	-	-	B_NVR1 V63[4]	B_NVR1 V63[3]	B_NVR1 V63[2]	B_NVR1 V63[1]	B_NVR1 V63[0]	
7th Parameter	1	↑	1	-	-	-	-	B_NVR2 V13[4]	B_NVR2 V13[3]	B_NVR2 V13[2]	B_NVR2 V13[1]	B_NVR2 V13[0]	
8th Parameter	1	↑	1	-	-	-	-	B_NVR2 V50[4]	B_NVR2 V50[3]	B_NVR2 V50[2]	B_NVR2 V50[1]	B_NVR2 V50[0]	
9th Parameter	1	↑	1	-	-	-	-	-	B_NVR3 V4[3]	B_NVR3 V4[2]	B_NVR3 V4[1]	B_NVR3 V4[0]	
10th Parameter	1	↑	1	-	-	-	-	-	B_NVR3 V8[3]	B_NVR3 V8[2]	B_NVR3 V8[1]	B_NVR3 V8[0]	
11th Parameter	1	↑	1	-	-	-	-	-	B_NVR3 V20[3]	B_NVR3 V20[2]	B_NVR3 V20[1]	B_NVR3 V20[0]	
12th Parameter	1	↑	1	-	-	-	-	-	B_NVR3 V27[3]	B_NVR3 V27[2]	B_NVR3 V27[1]	B_NVR3 V27[0]	
13th Parameter	1	↑	1	-	-	-	-	-	B_NVR3 V36[3]	B_NVR3 V36[2]	B_NVR3 V36[1]	B_NVR3 V36[0]	
14th Parameter	1	↑	1	-	-	-	-	-	B_NVR3 V43[3]	B_NVR3 V43[2]	B_NVR3 V43[1]	B_NVR3 V43[0]	
15th Parameter	1	↑	1	-	-	-	-	-	B_NVR3 V55[3]	B_NVR3 V55[2]	B_NVR3 V55[1]	B_NVR3 V55[0]	
16th Parameter	1	↑	1	-	-	-	-	-	B_NVR3 V59[3]	B_NVR3 V59[2]	B_NVR3 V59[1]	B_NVR3 V59[0]	

NOTE: "-" Don't care

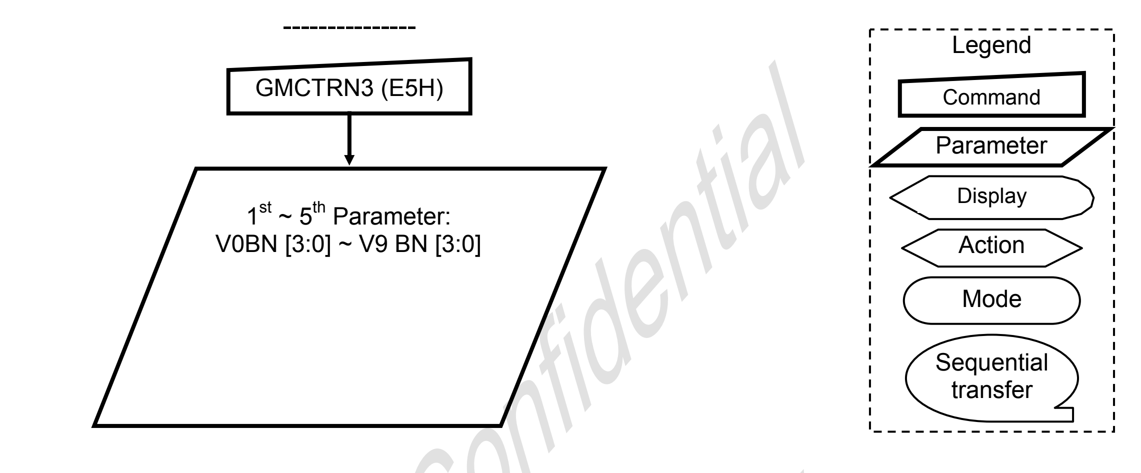
Description	-When turn ON the separate RGB gamma function the command is only used for **B gamma** ('-' polarity) of GC0 correction characteristics setting -When turn OFF the separate RGB gamma function the command is not used.
Restriction	
Register Availability	(see table below)
Default	(see table below)

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	----
S/W Reset	----
H/W Reset	----

Flow Chart	

GMCTRN3 (E5H)
1st ~ 5th Parameter:
V0BN [3:0] ~ V9 BN [3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7. FUNCTION DESCRIPTION

7.1. MCU & RGB Interface

The SPFD54126B features System interfaces and RGB interface to satisfy various needs of small or medium size's LCD panel. Based on the application requirements, there are two display modes mostly used in the LCD end product.

1. Still picture display mode
2. Moving picture display mode.

System interface is suitable for still picture display while RGB interface are suitable for moving picture display. Table 6.1 summarizes different interfaces for various display requirements.

Table 7.1 MCU & RGB Interface Comparisons table

Function	RCM1, RCM0				RCM1, RCM0			
Mode selection 1	"00"		"01"		"10"		"11"	
	8080/ 6800 IF + SPI I/F				RGB I/F + SPI I/F			
	MCU Mode 1		MCU Mode 2		RGB Mode 1		RGB Mode 2	
Mode selection 2	IM2='1'	IM2='0'	IM2='1'	IM2='0'	ICM='0'	ICM='1'	ICM='0'	ICM='1'
	8080/ 6800 IF	SPI I/F	8080/ 6800 IF	SPI I/F	RGB-1 I/F + SPI I/F		RGB-2 I/F + SPI I/F	
Motion /Still selection	Motion or Still	Still	Motion or Still	Still	Motion or Still	Still	Motion or Stil	Still
Input data	D[B:0]	D0 = SDA	D[B:0]	SDA H/W pin	D[B:0]	SDA H/W pin	D[B:0]	SDA H/W pin
Input signal	CSX	D/CX = SCL	CSX	SCL H/W pin	PCLK	D/CX = SCL	PCLK	D/CX = SCL
	WRX (R/WX), RDX (E)	CSX	WRX (R/WX), RDX (E)	SPI_CSX	VS, HS, DE	CSX	VS, HS, DE	CSX
GRAM Write cycle	Refer WRX	Refer SCL	Refer WRX	Refer SCL	Refer PCLK	Refer SCL	Refer PCLK	Refer SCL
GRAM Read Cycle	Refer Internal Oscillator		Refer Internal Oscillator		Refer PCLK	Refer Internal Oscillator	Refer PCLK	Refer Internal Oscillator
Command setting	D[7:0]	D0 = SDA	D[7:0]	SDA H/W pin	SDA	SDA H/W pin	SDA	SDA H/W pin
SMX, SMY, SRGB	-When Power On or H/W reset, those function follow H/W pins setting first.							
VSYNC I/F	-By command setting -Default is OFF		-By command setting -Default is ON		-No support this function in these modes			
TE Function					-By command setting			
Normal / Partial mode	-By command setting				-By command setting			
Idle Mode (IDM H/W pin)	-By command setting -Don't care in this mode, but should be set to VDDI or DGND.						-By IDM H/W pin -IDM On/OFF (39H/28H) are disable	
Display On/ Off (SHUT H/W pin)							-By SHUT H/W pin -SLPIN(10H), SLPOUT(11H), Display On/OFF (29h/28H) are disable	
Data inverter (REV H/W pin)							-By REV H/W pin -INVON/OFF (21H/20H) are disable	
DE H/W pin	-Don't care in this mode, but should be set to VDDI or DGND				-The data latched by rising edge of PCLK when DE='1' -When display data coming the DE signal should be VDDI level		-When DE='0' area, output is blanking display	
RL H/W pin					-Don't care in this mode, but should be set to VDDI or DGND		-By H/W pin -No commands conflict	
TB H/W pin								
Blanking porch	-Don't care in this mode				-Control by DE signal		-Control by RGBBPCTR (D5)	
Colors Format	-Control by **IFPF[2:0]** of COLMOD(3AH)				-Control by **VIPF[3:0]** of COLMOD (3AH)			

Note 1: RCM1 and RCM0 are H/W setting pins.

Note 2: In RGB + SPI I/F (RCM="1x"), VS, HS, DE, PCLK and D[17:0] are Hi-Z by Driver and can be stop for Host, when ICM='1'.

Note 3: In RGB + SPI I/F (RCM="1x"), the data deliver via GRAM

Note 4: When Power on Driver IC should be detect SMX, SMY, SRGB H/W setting

Note 5: When Power on Driver IC should be detect RCM1, RCM0 H/W setting and get into the I/F mode.

Note 6: When Power on Driver IC should be detect LCM1, LCM0 H/W setting and get into the setting mode.

Note 7: When Power on Driver IC should be detect GM1, GM0 H/W setting and get into the setting mode.

7.2. MPU Interface

7.2.1. Interface Type Selection

The MPU interfaces of SPFD54126B support 8-bit, 9-bit, 16-bit, and 18-bit's 80- or 68-system Interface and Serial Peripheral Interface (SPI), which can be set by the P68 and IM2/1/0 pins. The MPU interface can set instructions and access RAM. Table 6.2.1 depicts the interface corresponding to P68and IM2/1/0 settings.

Table 7.2.1

P68	IM2	IM1	IM0	Interface	Read back selection
0	0	-	-	3-Pin Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter
0	1	0	0	8080 MCU 8-bits Parallel	RDX strobe (8-bits read data and 8-bits read parameter)
0	1	0	1	8080 MCU 16-bits Parallel	RDX strobe (16-bits read data and 8-bits read parameter)
0	1	1	0	8080 MCU 9-bits Parallel	RDX strobe (9-bits read data and 8-bits read parameter)
0	1	1	1	8080 MCU 18-bits Parallel	RDX strobe (18-bits read data and 8-bits read parameter)
1	0	-	-	3-Pin Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter
1	1	0	0	6800 MCU 8-bits Parallel	E strobe (8-bits read data and 8-bits read parameter)
1	1	0	1	6800 MCU 16-bits Parallel	E strobe (16-bits read data and 8-bits read parameter)
1	1	1	0	6800 MCU 9-bits Parallel	E strobe (9-bits read data and 8-bits read parameter)
1	1	1	1	6800 MCU 18-bits Parallel	E strobe (18-bits read data and 8-bits read parameter)

7.2.2. 8080-Series Parallel interface(P68='0')

The MCU uses a 11-wires 8-data parallel interface or 19-wires 16-data parallel interface or 12-wires 9-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (DGND). Interface bus width can be selected with IM2, IM1 and IM0.

The interface function of 8080-series parallel interface are given in Table 6.2.2

Table 7.2.2 The function of 8080-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	1	0	0	8-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
					1	1	↑	Write 8-bits display data or 8-bits parameter (D7 to D0)
					1	↑	1	Read 8-bits command (D7 to D0)
					1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	1	0	1	16-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
					1	1	↑	Write 16-bits display data (D15 to D0) or 8-bits parameter (D7 to D0)
					1	↑	1	Read 8-bits command (D7 to D0)
					1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	1	1	0	9-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
					1	1	↑	Write 9-bits display data (D8 to D0) or 8-bits parameter (D7 to D0)
					1	↑	1	Read 8-bits command (D7 to D0)
					1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	1	1	1	18-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
					1	1	↑	Write 18-bits display data (D17 to D0) or 8-bits parameter (D7 to D0)
					1	↑	1	Read 8-bits command (D7 to D0)
					1	↑	1	Read 8-bits parameter or status (D7 to D0)

7.2.2.1. Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

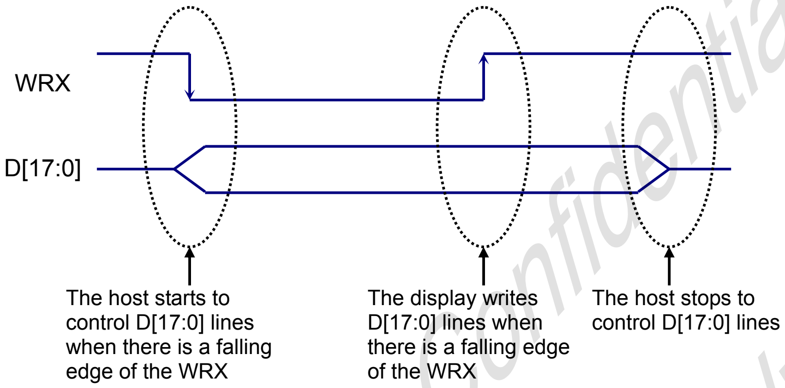


Fig. 7.2.2.1.1 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped)

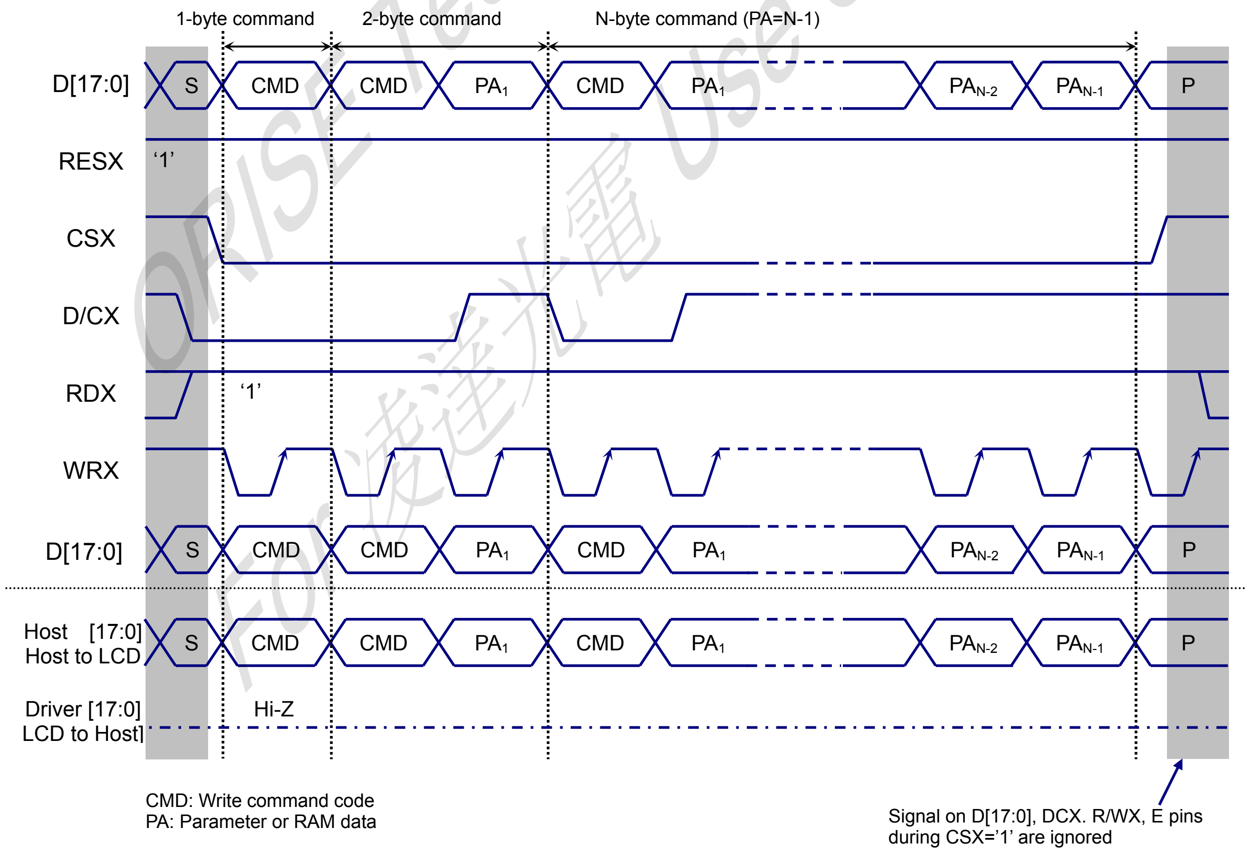


Fig. 7.2.2.1.2 8080-Series parallel bus protocol, Write to register or display RAM

7.2.2.2. Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

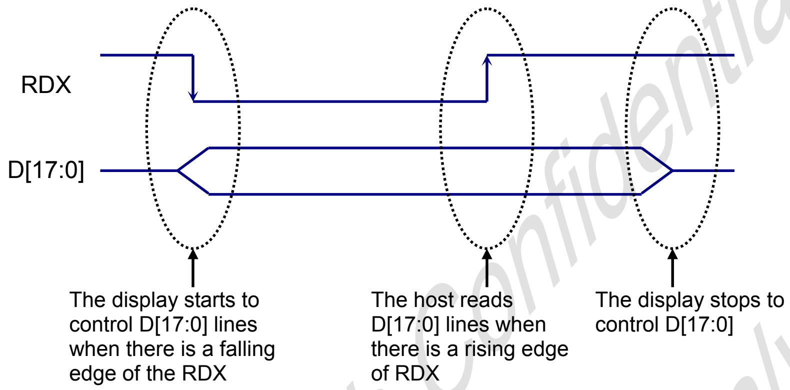


Fig. 7.2.2.2.1 8080-Series RDX Protocol

Note: RDX is an unsynchronized signal (It can be stopped)

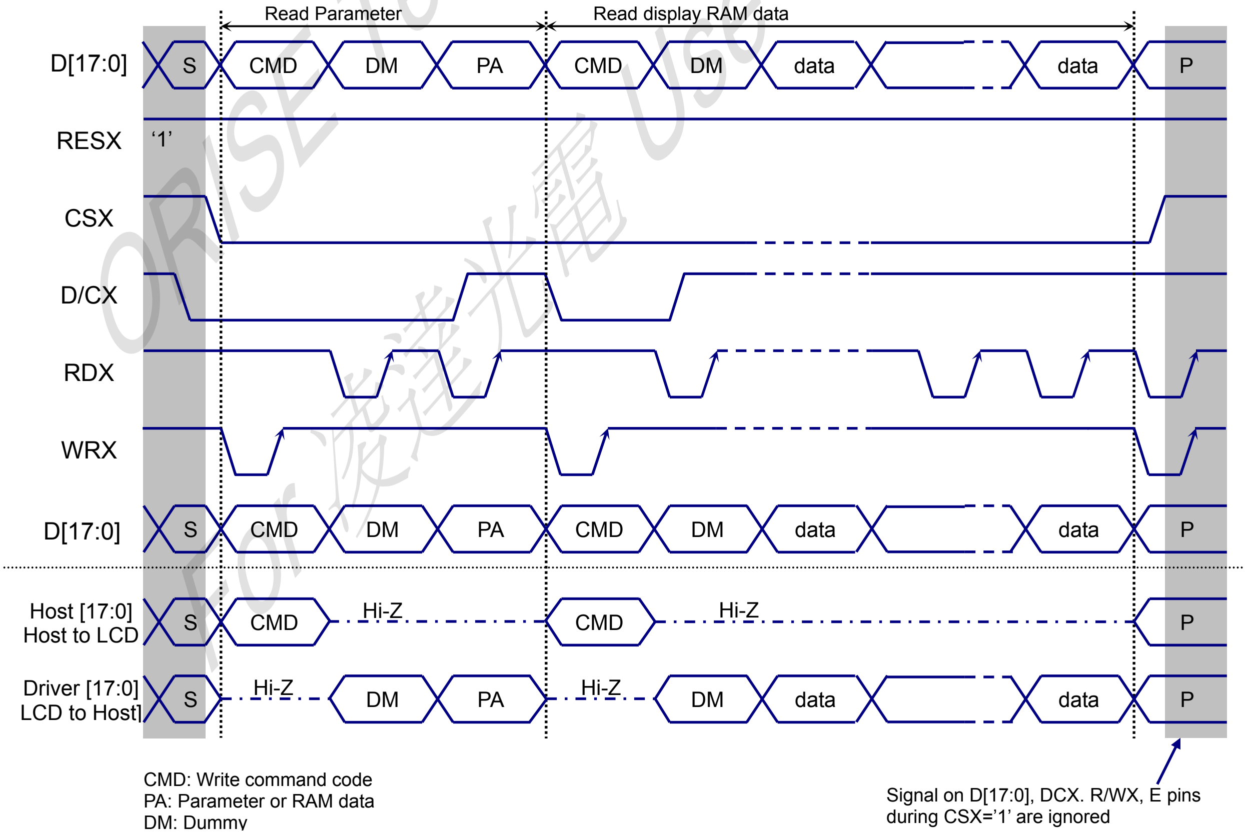


Fig. 7.2.2.2.2 8080-Series parallel bus protocol, Read data from register or display RAM

7.2.3. 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-wires 8-data parallel interface or 19-wires 16-data parallel interface or 12-wires 9-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of E signal when R/WX='1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 6800-series parallel interface are given in Table 7.2.3.

Table 7.2.3 The function of 6800-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bits Parallel	0	0	↓	Write 8-bits command (D7 to D0)
					1	0	↓	Write 8-bits display data or 8-bits parameter (D7 to D0)
					1	1	↓	Read 8-bits command (D7 to D0)
					1	1	↓	Read 8-bits parameter or status (D7 to D0)
1	1	0	1	16-bits Parallel	0	0	↓	Write 8-bits command (D7 to D0)
					1	0	↓	Write 16-bits display data (D15 to D0) or 8-bits parameter (D7 to D0)
					1	1	↓	Read 8-bits command (D7 to D0)
					1	1	↓	Read 8-bits parameter or status (D7 to D0)
1	1	1	0	9-bits Parallel	0	0	↓	Write 8-bits command (D7 to D0)
					1	0	↓	Write 9-bits display data (D8 to D0) or 8-bits parameter (D7 to D0)
					1	1	↓	Read 8-bits command (D7 to D0)
					1	1	↓	Read 8-bits parameter or status (D7 to D0)
1	1	1	1	18-bits Parallel	0	0	↓	Write 8-bits command (D7 to D0)
					1	0	↓	Write 18-bits display data (D17 to D0) or 8-bits parameter (D7 to D0)
					1	1	↓	Read 8-bits command (D7 to D0)
					1	1	↓	Read 8-bits parameter or status (D7 to D0)

7.2.3.1. Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

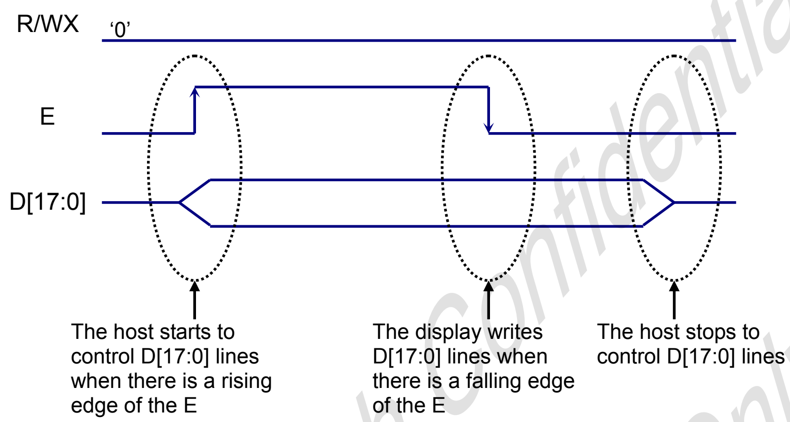


Fig. 7.2.3.1.1 6800-Series Write Protocol

Note: E is an unsynchronized signal (It can be stopped)

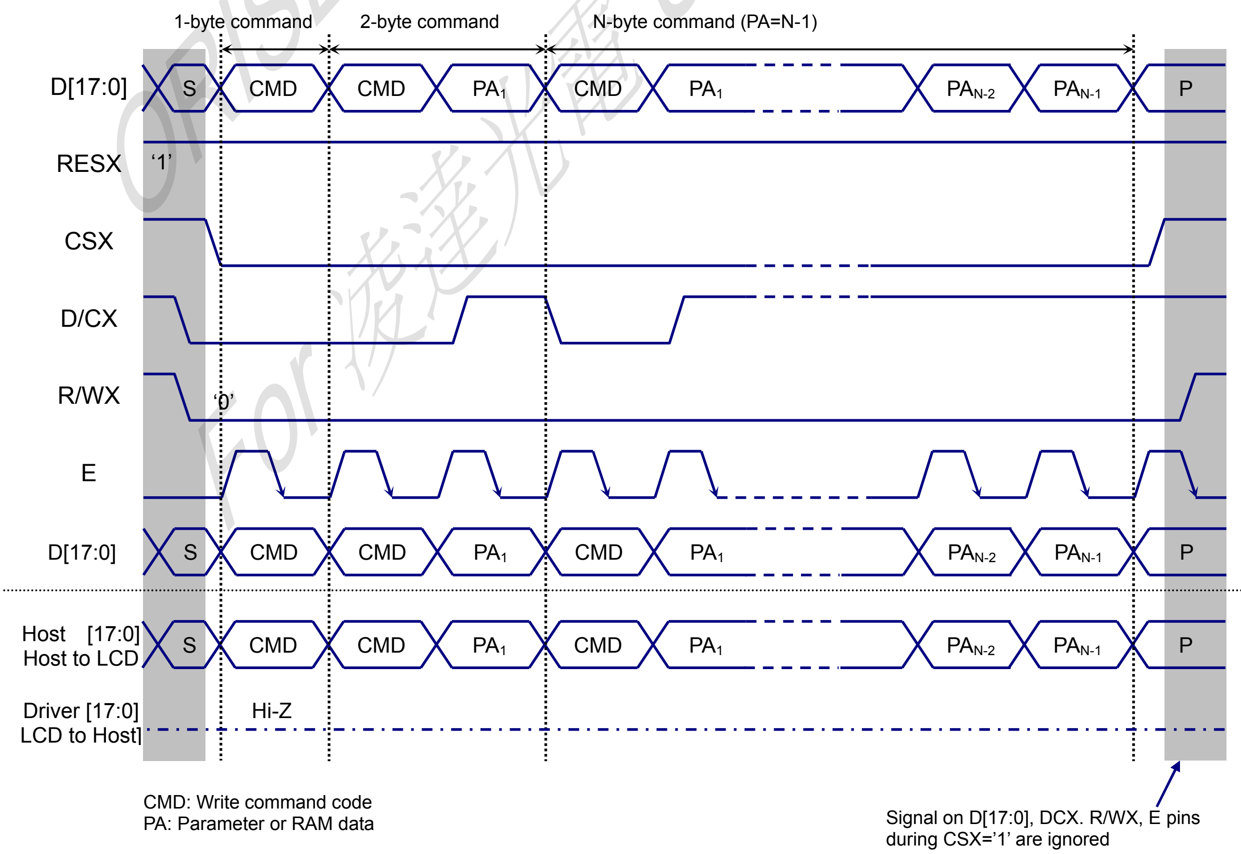


Fig. 7.2.3.1.2 6800-Series parallel bus protocol, Write to register or display RAM

7.2.3.2. Read cycle sequence

The read cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

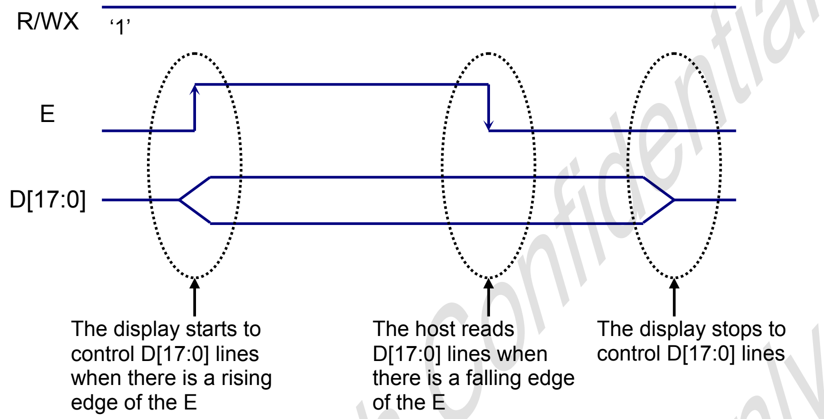


Fig. 7.2.3.2.1 6800-Series Read Protocol

Note: E is an unsynchronized signal (It can be stopped)

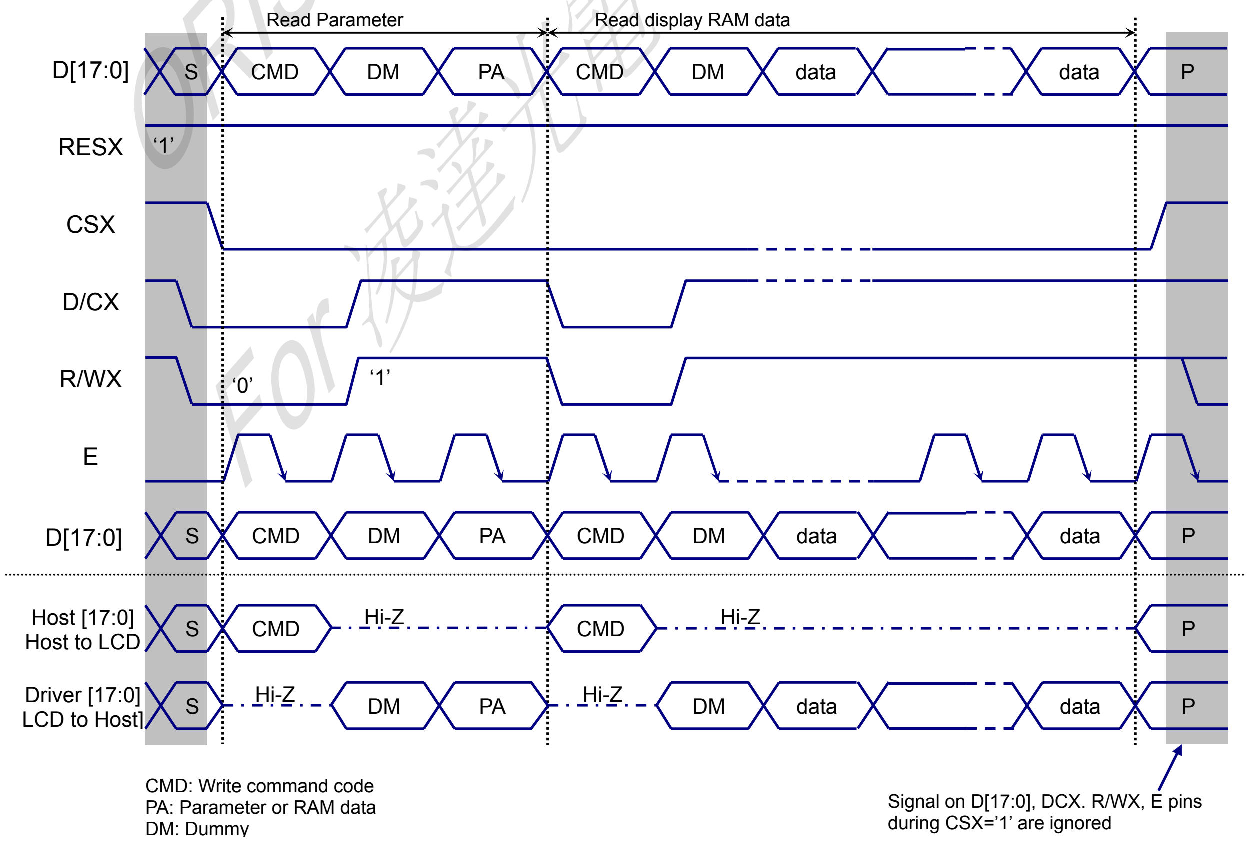


Fig. 7.2.3.2.2 6800-Series parallel bus protocol, Read data from register or display RAM

7.2.4. Serial Peripheral interface (SPI)

The selection of this interface is done by IM2. See the Table 7.2.4.

The serial interface is a 3-pin 9-bits bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Table 7.2.4 Serial Interface Type Selection

P68	IM2	IM1	IM0	Interface	Read back selection
‘-‘	0	‘-‘	‘-‘	3-Pin Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter

7.2.4.1. Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the 3-Pin serial data packet contains a control bit D/CX and a transmission byte. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the DRIVER. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

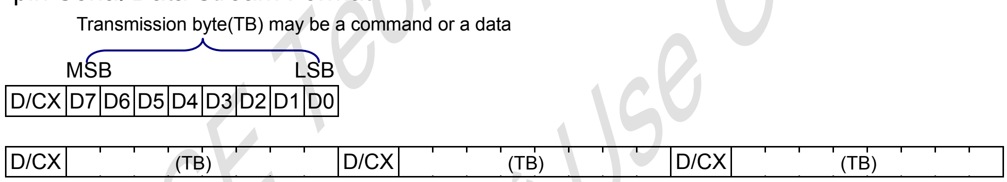


Fig. 7.2.4.1.1 Serial interface data Stream format

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX=’0’) or parameter/RAM data (D/CX=’1’). It is sampled when first rising edge of CSX. If CSX stay low after the last bit of command/data byte, the serial interface expects the D/CX bit of the next byte at the next rising edge of SCL.

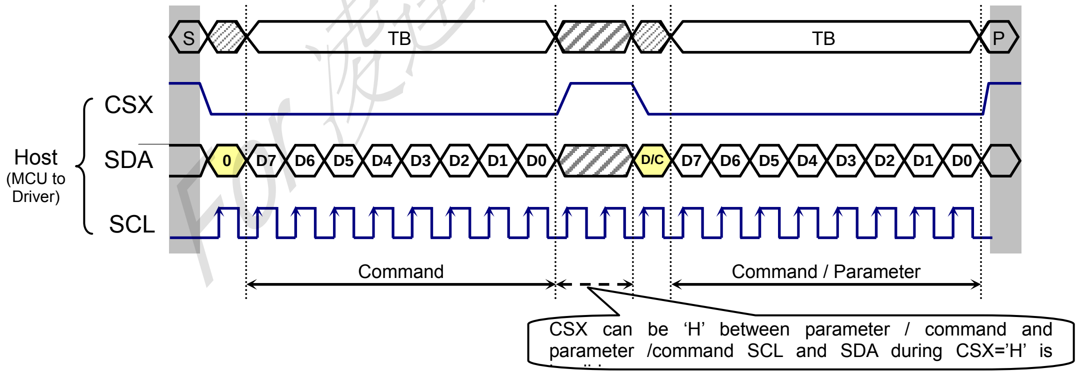
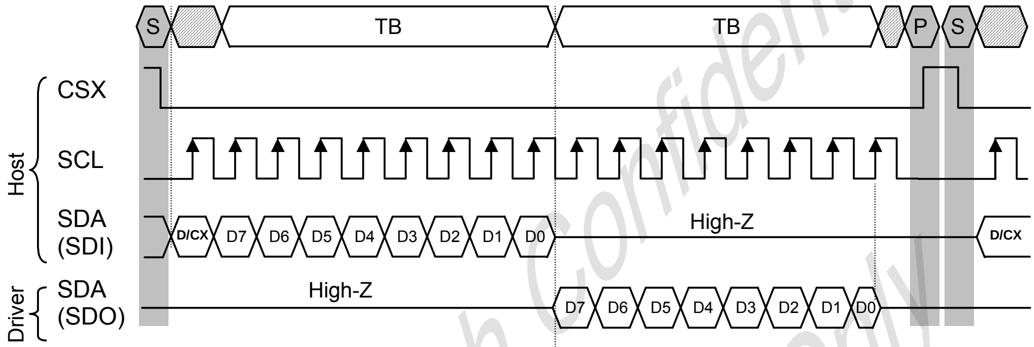


Fig. 7.2.4.1.2 Serial interface Write protocol (Write to register with control bit in transmission)

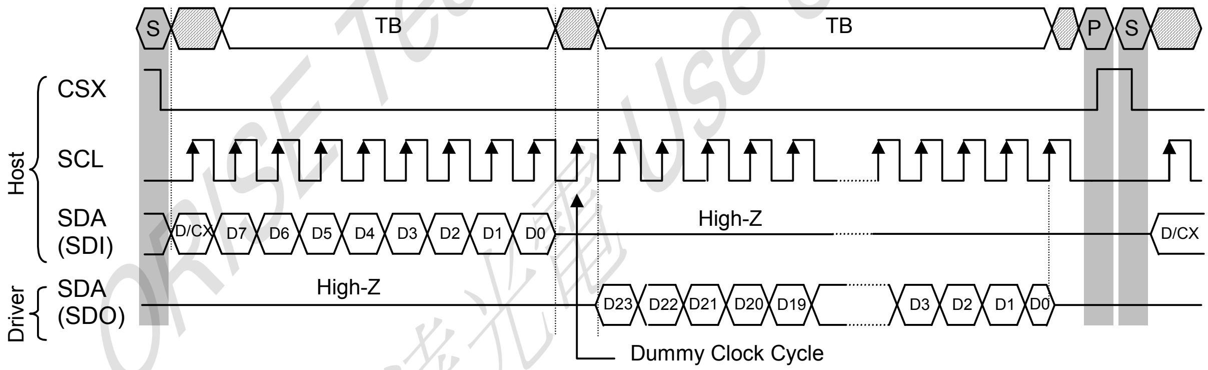
7.2.4.2. Read Functions

The read mode of the interface means that the micro controller reads register value from the Driver. To do the micro controller first has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. After the read status command has been sent, the SDA lin must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-Pin Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



3-Pin Serial Protocol (for RDDID command: 24-bit read)



3-Pin Serial Protocol (for RDDST command: 32-bit read)

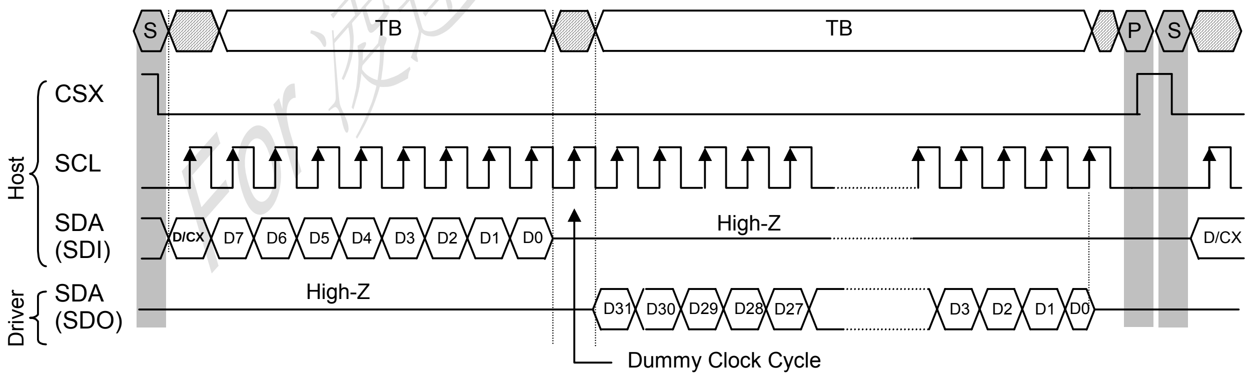


Fig. 7.2.4.2.1 3-pin Serial interface Read protocol

7.2.5. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example

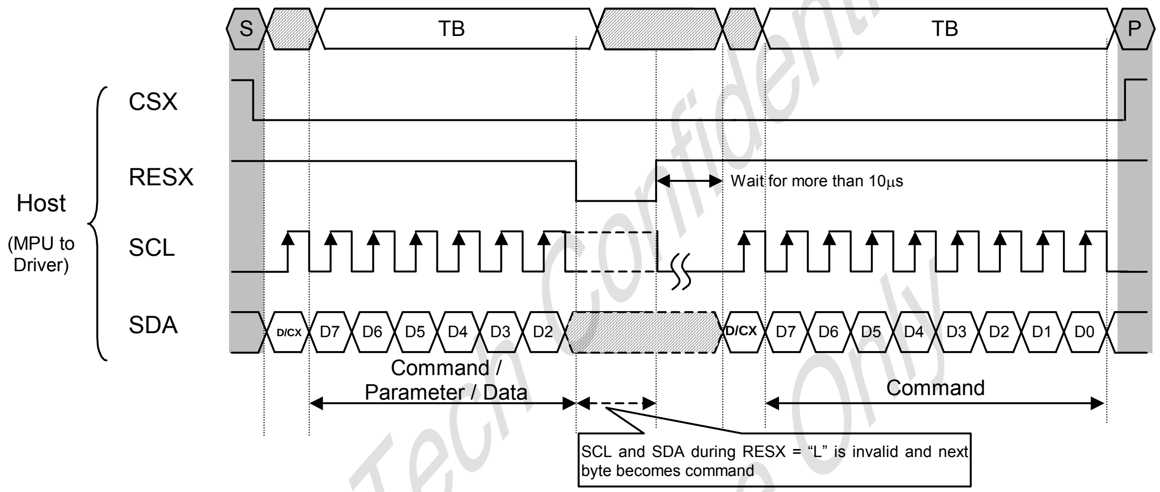


Fig. 7.2.5.1 Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

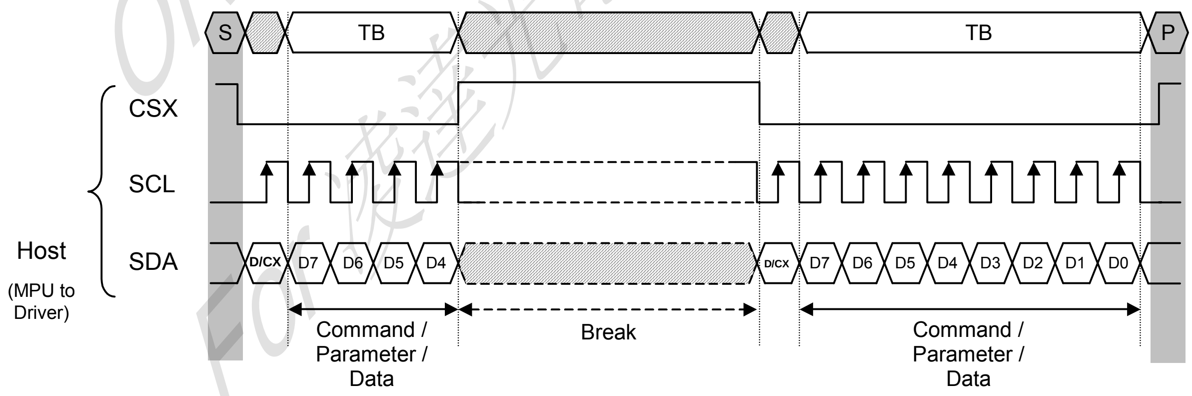


Fig. 7.2. 5.2 Serial bus protocol, write mode – interrupted by CSX

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

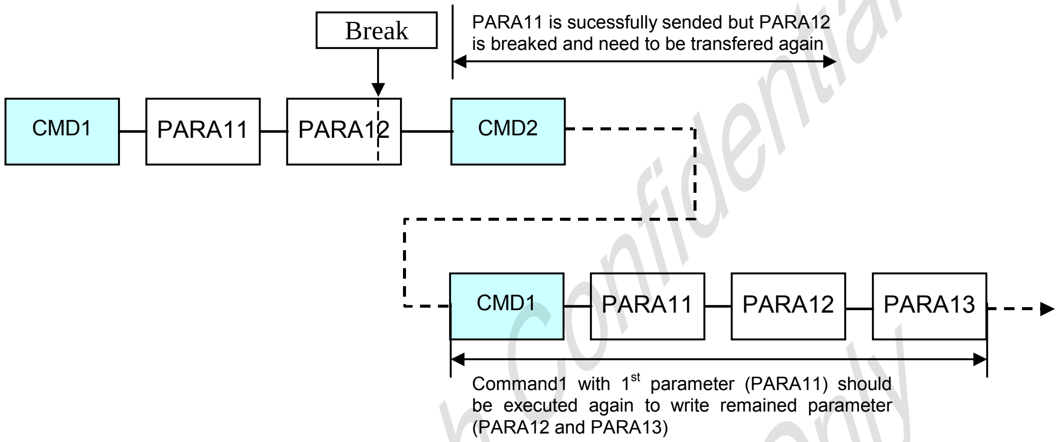


Fig.7.2.5.3 Write interrupts recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

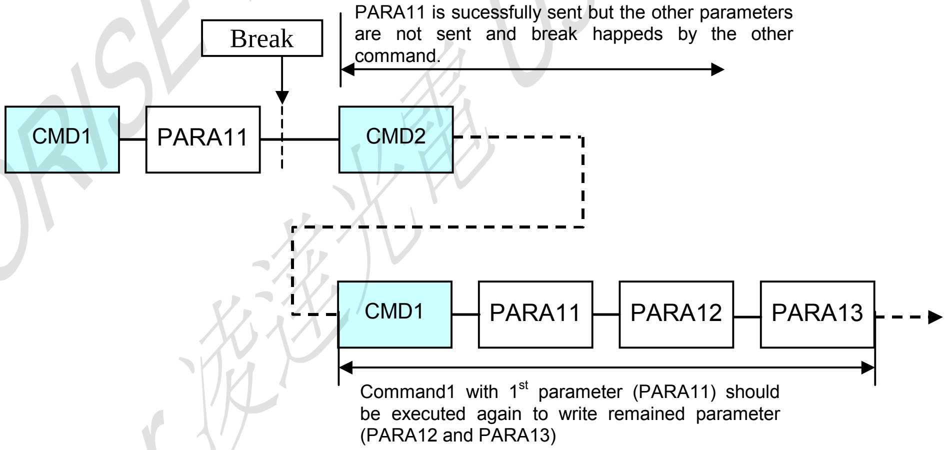


Fig. 7.2.5.4 Write interrupts recovery (both serial and parallel interface)

7.2.6. Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then DRIVER will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command

2) Command-Pause-Parameter

3) Parameter-Pause-Command

4) Parameter-Pause-Parameter

7.2.6.1. Serial Interface Pause

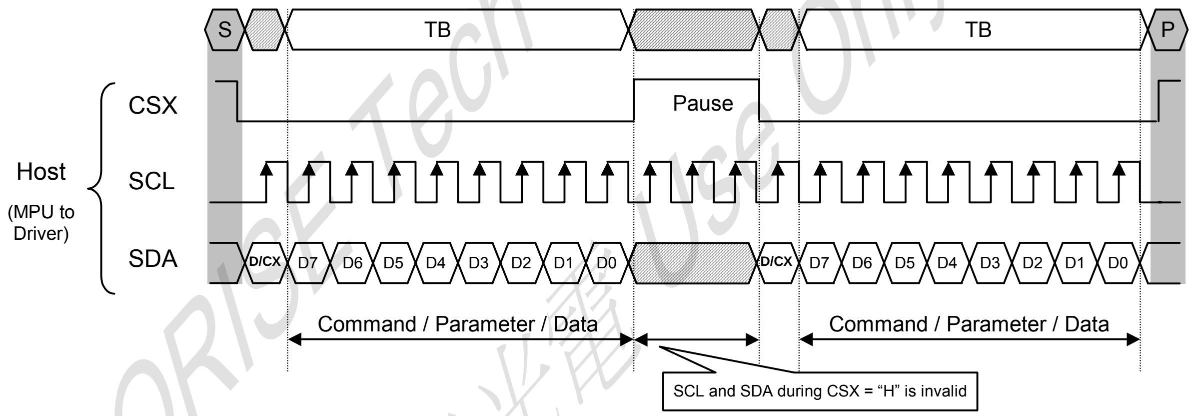


Fig. 7.2.6.1 Serial interface Pause Protocol (pause by CSX)

7.2.6.2. Parallel Interface Pause

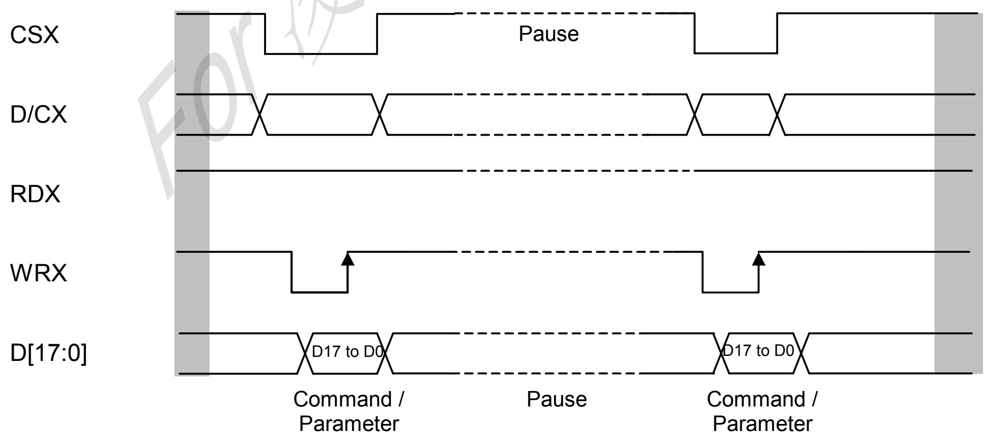


Fig. 7.2.6.2 Parallel bus Pause Protocol (paused by CSX)

7.2.7. Data Transfer Modes

The Module has three kinds colour modes for transferring data to the display RAM. These are 12-bit colour per pixel, 16-bit colour per pixel and 18-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

7.2.7.1. Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

Start					Stop
Start Frame Memory Write	Image Data Frame 1	Image Data Frame 2	Image Data Frame 3	....	Any Command

7.2.7.2. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.

Start						
Start Frame Memory Write	Image Data Frame 1	Any Command	Start Frame Memory Write	Image Data Frame 2	Any Command	....

	Stop
....	Any Command

Note:

1) These apply to all data transfer Colour modes on both serial and parallel interfaces.

2) The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.3. MCU Data Colour Coding

7.3.1. MCU Data Colour Coding for RAM data *Write*

- Parallel 8-Bits Bus Interface (IM1, IM0= "00")

Table 7.3.1.1 8-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
03h	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	4K-Colour (2-pixels/ 3-byyes)
	x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	
05h	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Colour (1-pixels/ 2-byyes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Colour (1-pixels/ 3byyes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

- Parallel 16-Bits Bus Interface (IM1, IM0= "01")

Table 7.3.1.2 16-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Colour
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Colour
06h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Colour (2-pixels/ 3byyes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

- Parallel 9-Bits Bus Interface (IM1, IM0= "10")

Table 7.3.1.3 9-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
06h	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Colour (1-pixels/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

- Parallel 18-Bits Bus Interface (IM1, IM0= "11")

Table 7.3.1.4 18-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	**4K-Colour**
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	**65K-Colour**
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Colour**

Note: 'x' Don't care, but need to set VDDI or DGND level.

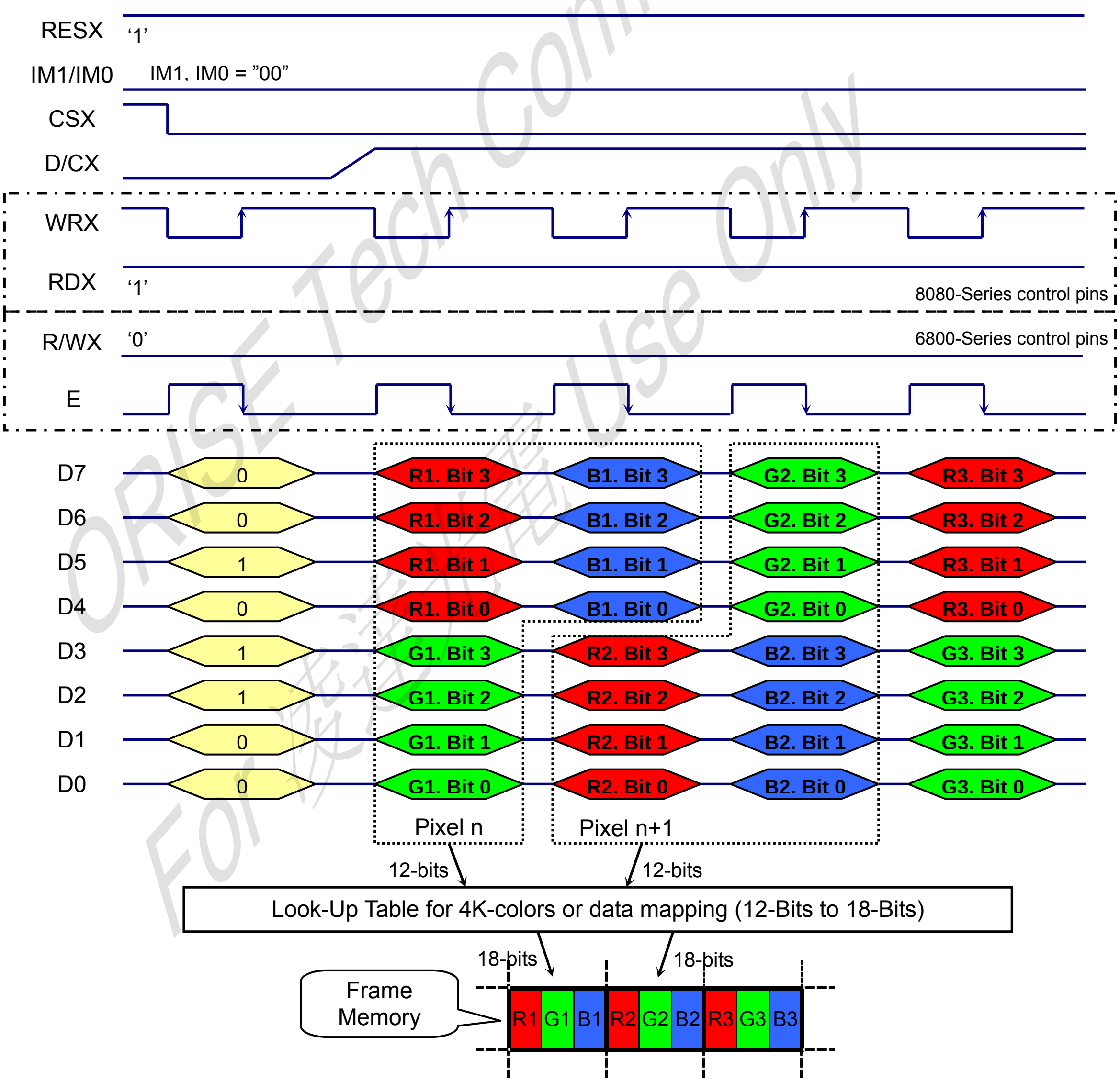
7.3.1.1. Parallel 8-Bits Bus Interface for RAM Data Write (IM1, IM0= "00")

Different display data formats are available for three colours depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 8-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"

There are 2 pixels (6 sub-pixels) per 3-bytes.



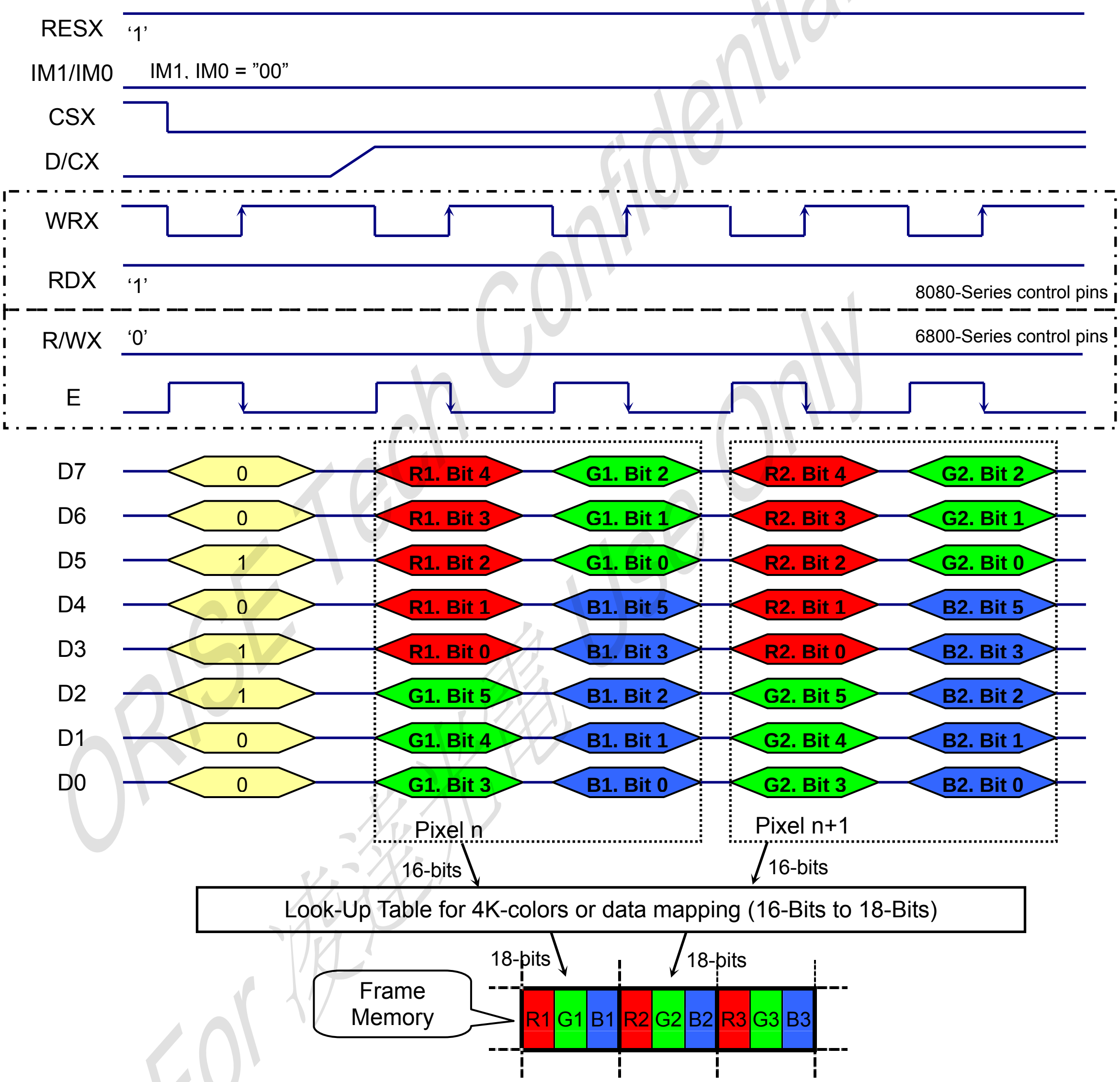
Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

(2). 8-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"

There are 1 pixels (3 sub-pixels) per 2-bytes.



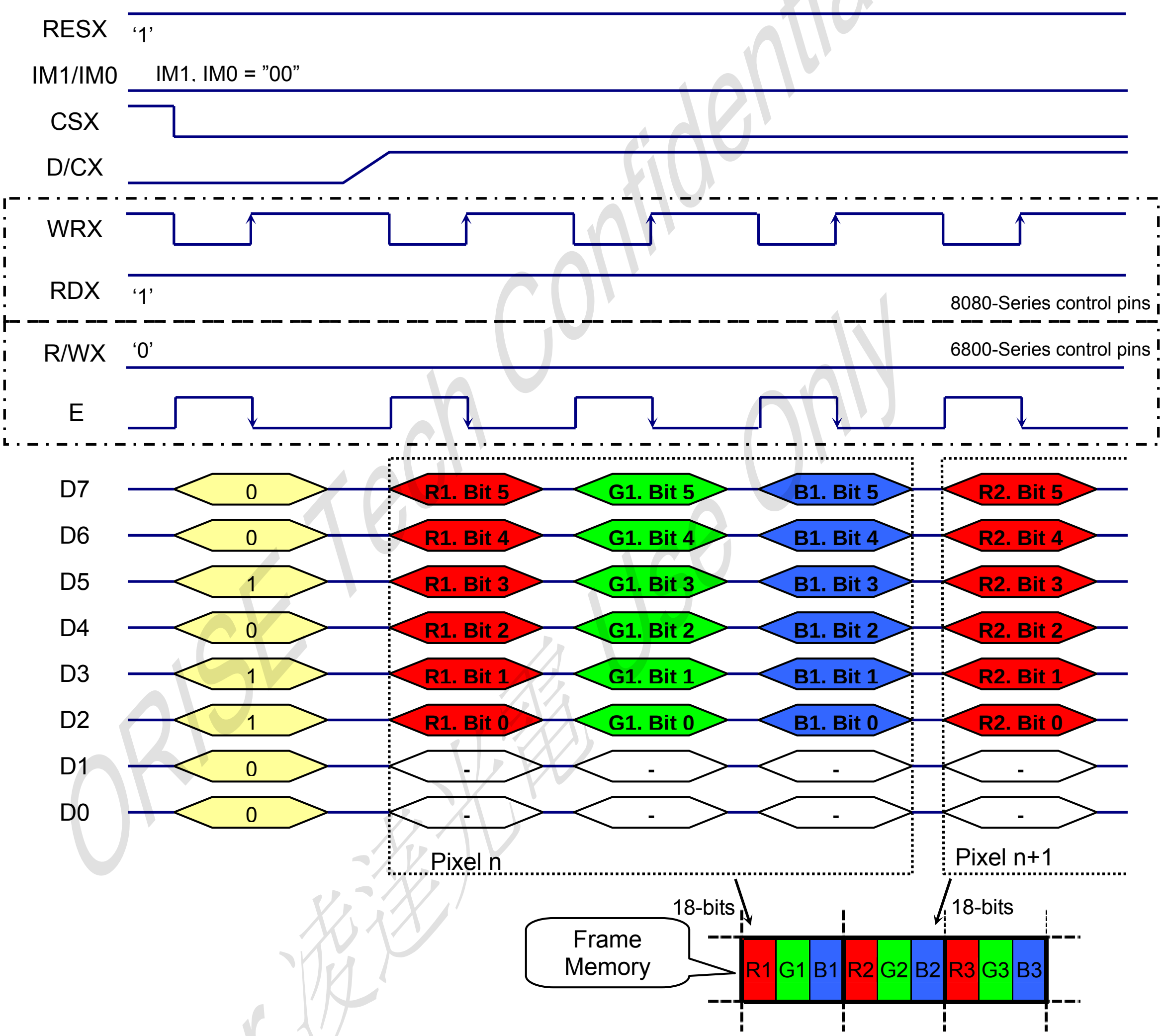
Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

(3). 8-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 1 pixels (3 sub-pixels) per 3-bytes.



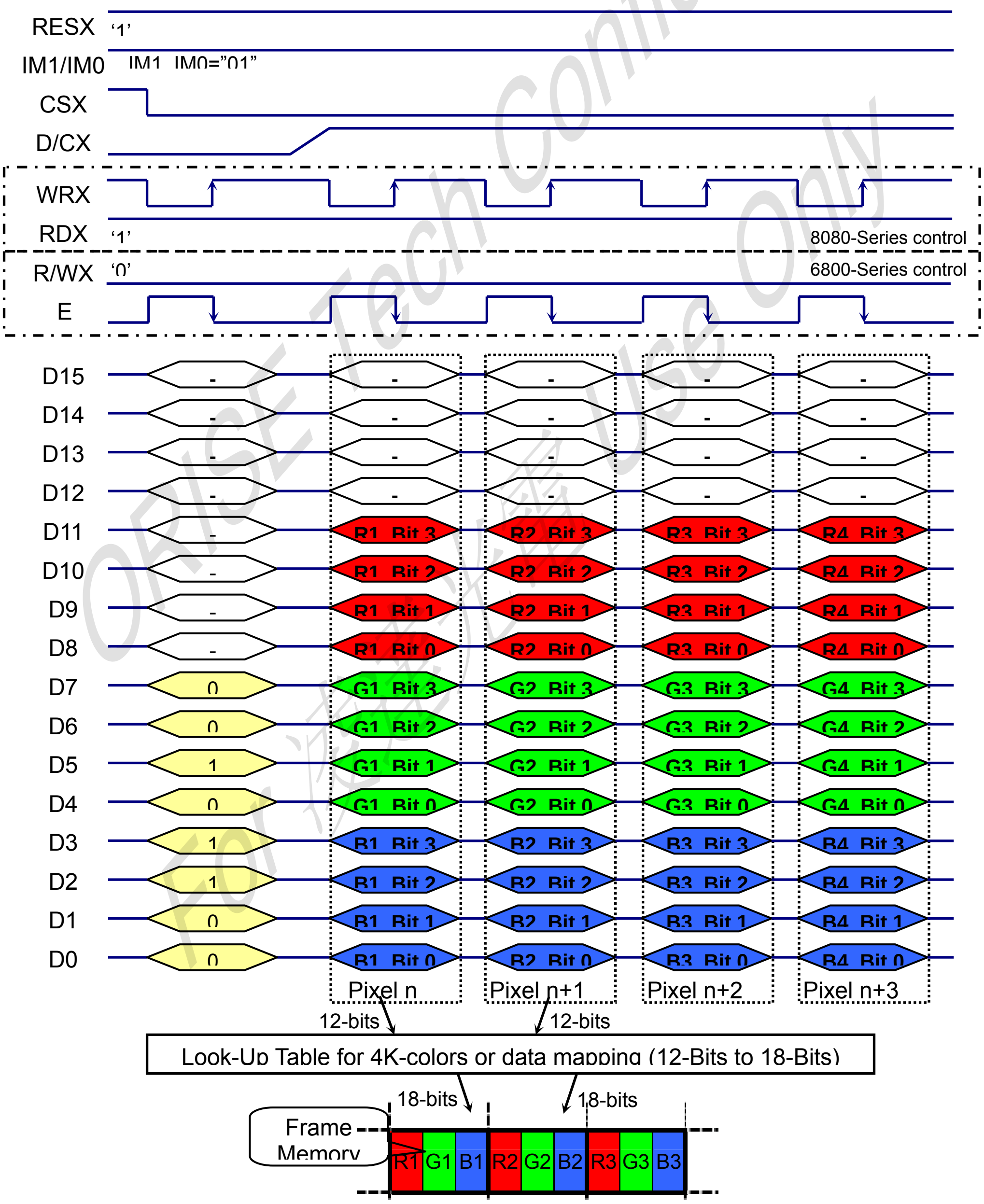
7.3.1.2. Parallel 16-Bits Bus Interface for RAM Data Write (IM1, IM0="01")

Different display data formats are available for three colors depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 16-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"

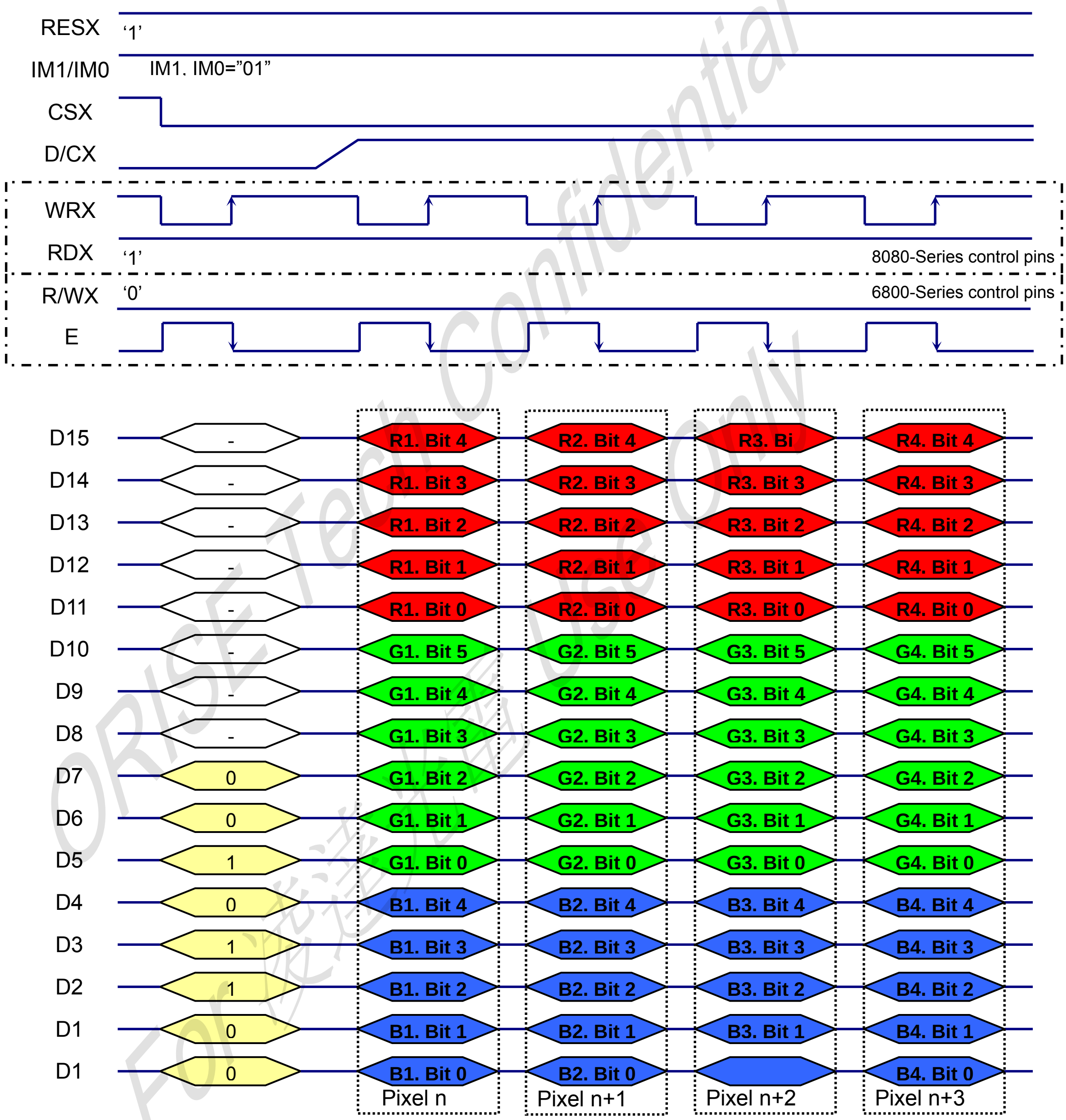
There are 1 pixel (3 sub-pixels) per 1 bytes

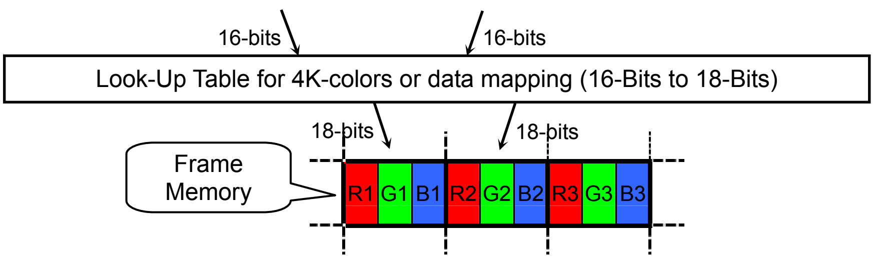


Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.
Note 3. '-' = Don't care - Can be set to VDDI or DGND level

(2). 16-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"

There are 1 pixel (3 sub-pixels) per 1 bytes





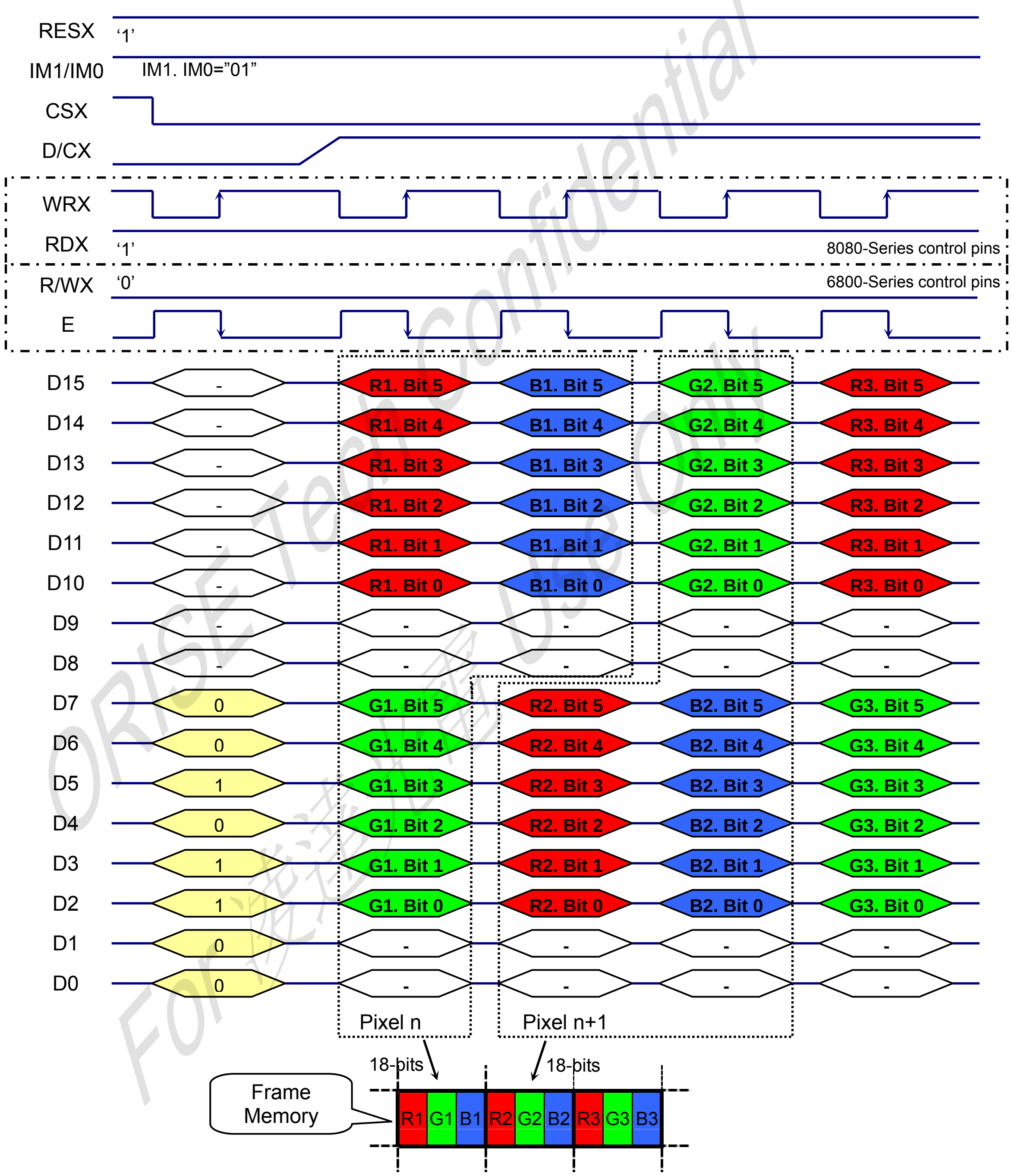
Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

(3). 16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 2 pixel (6 sub-pixels) per 3 bytes



Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

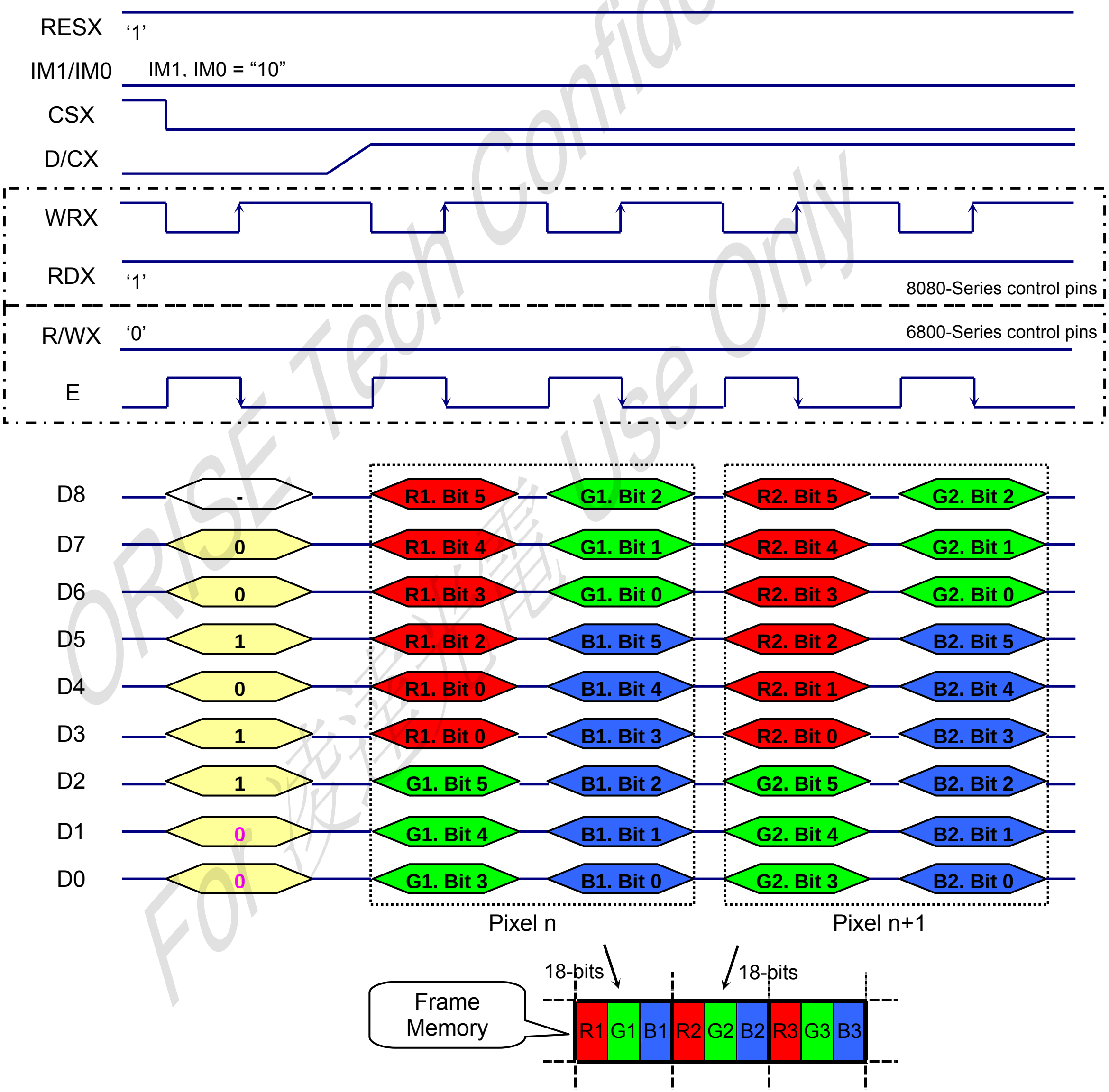
7.3.1.3. Parallel 9-Bits Bus Interface for RAM Data Write (IM1, IM0="10")

Different display data formats are available for three colors depth supported by listed below.

- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 9-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 2 bytes



Note1. The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

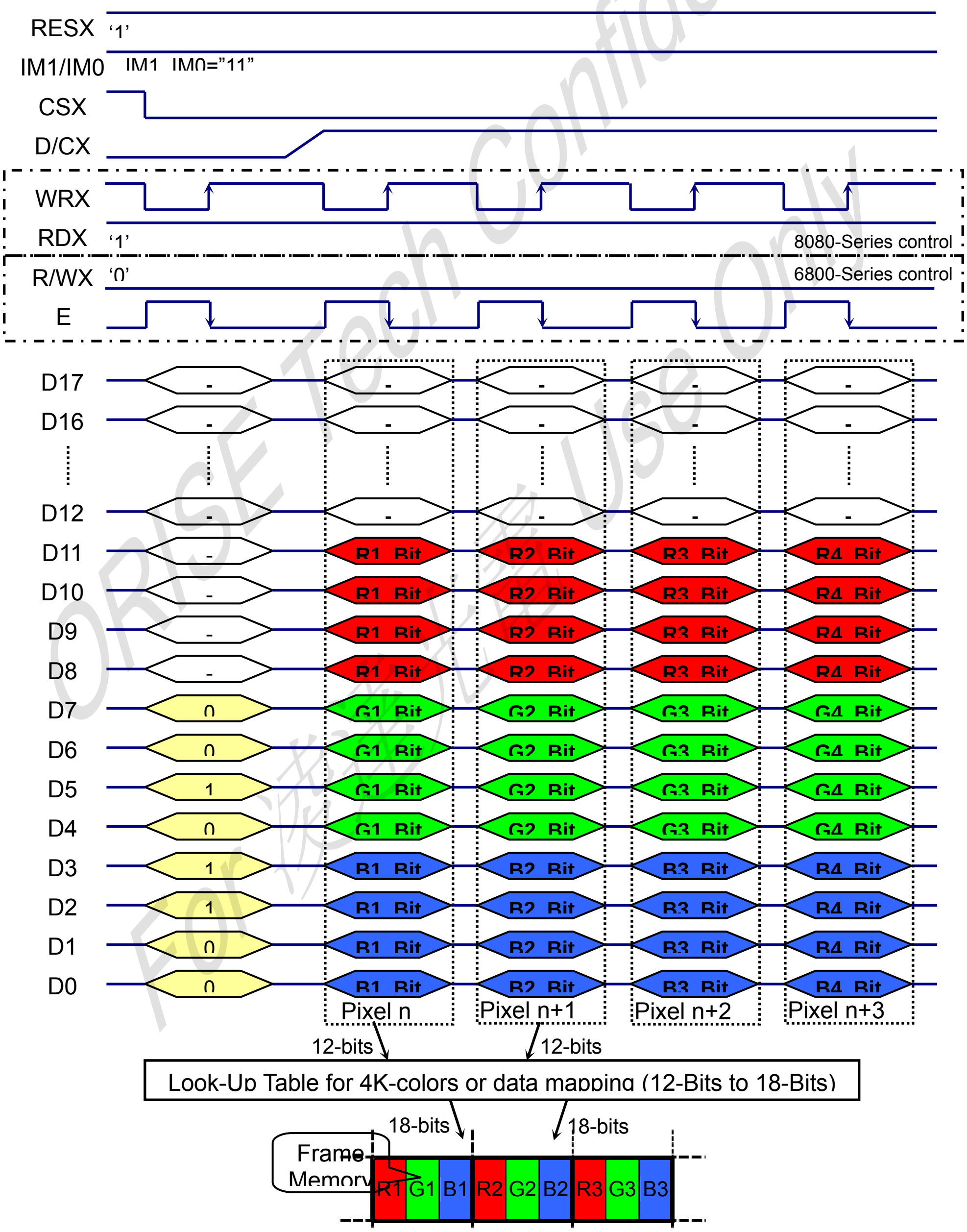
7.3.1.4. Parallel 18-Bits Bus Interface for RAM Data Write (IM1, IM0="11")

Different display data formats are available for three colors depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 18-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"

There is 1 pixel (3 sub-pixels) per 1 bytes



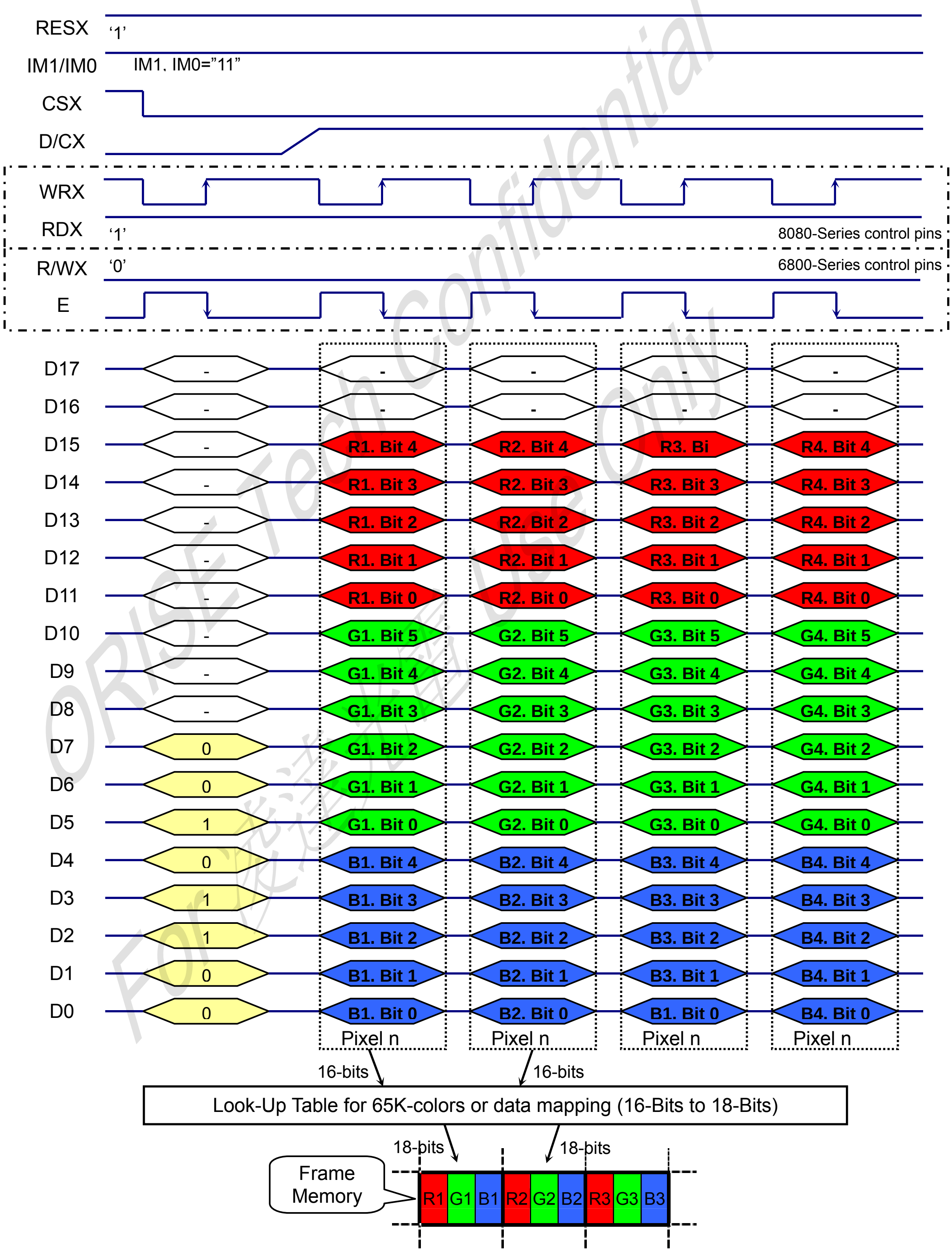
Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

(2). <u>18-bits data bus</u> for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, <u>3AH="05h"</u>

There are 1 pixel (3 sub-pixels) per 1 bytes



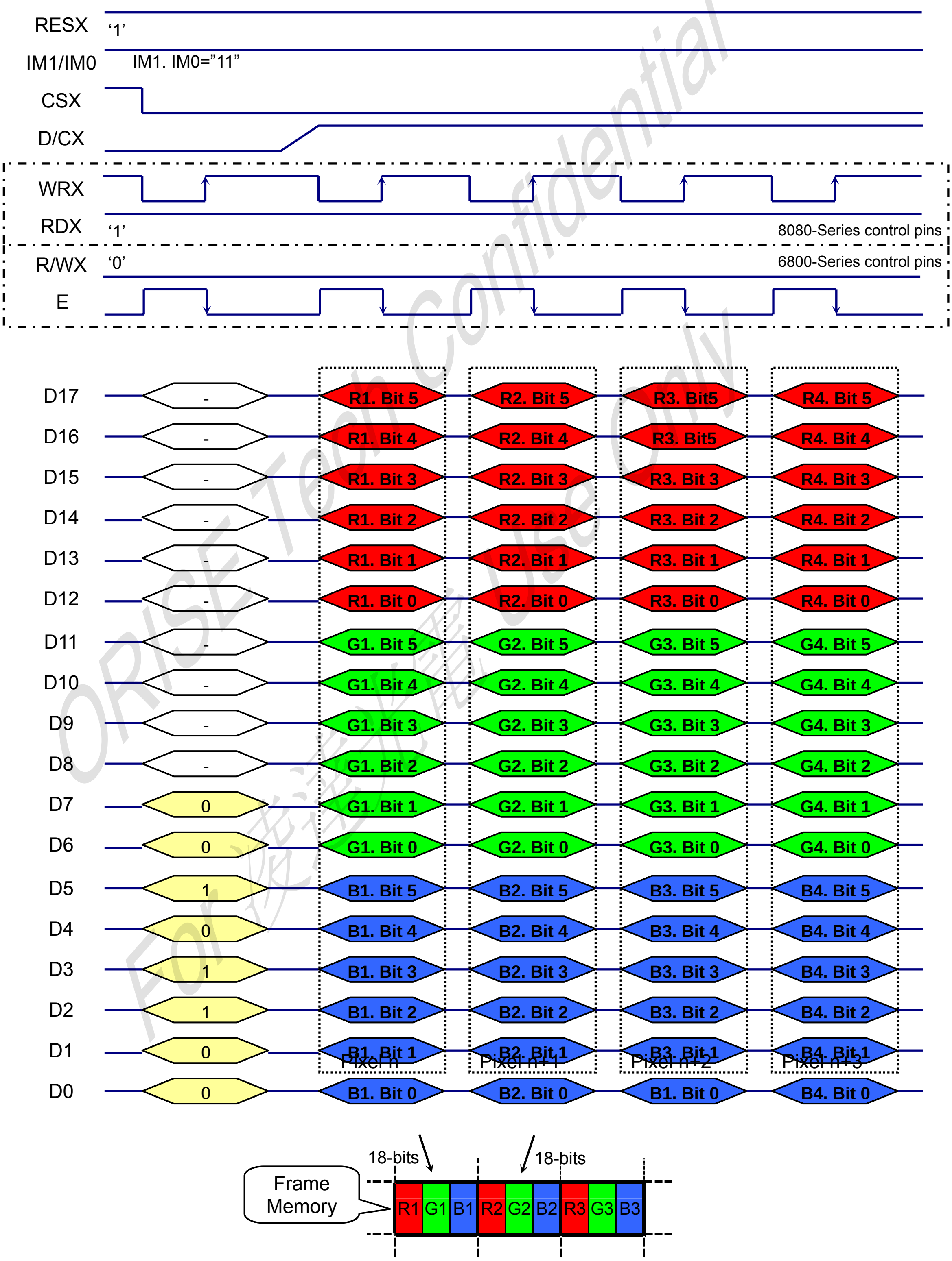
Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

(3). 18-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 1 pixel (6 sub-pixels) per 1 bytes



Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

7.3.2. MCU Data Colour Coding for RAM data ***Read***

- Parallel 8-Bits Bus Interface (IM1, IM0= "00")

Table 7.3.2.1 8-Bits Parallel Interface Set Table

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Colour (1-pixels/ 3byyes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

- Parallel 16-Bits Bus Interface (IM1, IM0= "01")

Table 7.3.2.2 16-Bits Parallel Interface Set Table

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Colour (2-pixels/ 3byyes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

- Parallel 9-Bits Parallel Interface (IM1, IM0= "10")

Table 7.3.2.3 9-Bits Parallel Interface Set Table

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Colour (1-pixels/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

- Parallel 18-Bits Parallel Interface (IM1, IM0= "11")

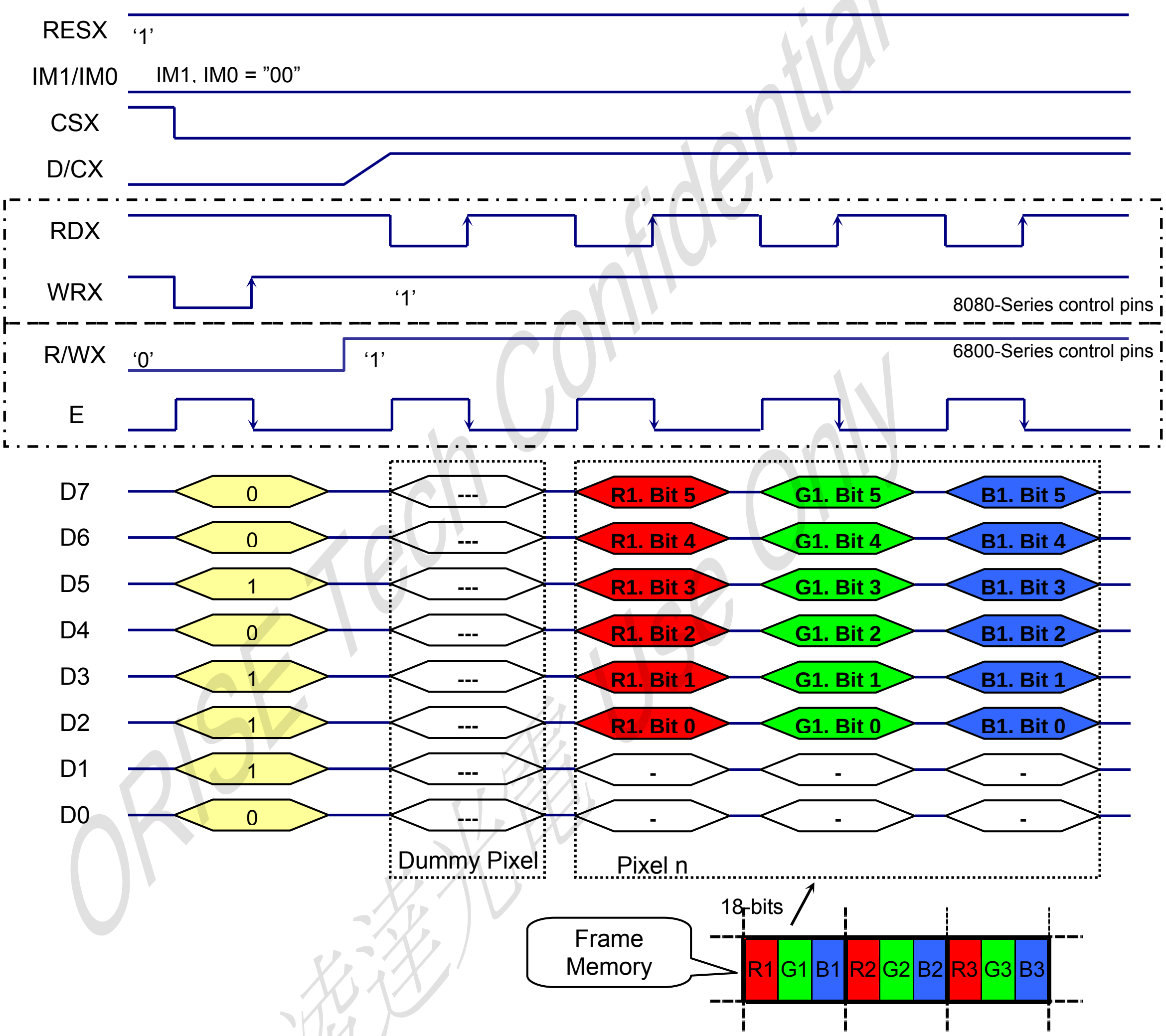
Table 7.3.2.4 18-Bits Parallel Interface Set Table

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Colour**

Note . 'x' Don't care, but need to set VDDI or DGND level.

7.3.2.1. Parallel 8-Bits Bus Interface for RAM Data Read (IM1, IM0= "00")

There are 1 pixels (3 sub-pixels) per 3-bytes. (RGB 6-6-6-bits output)



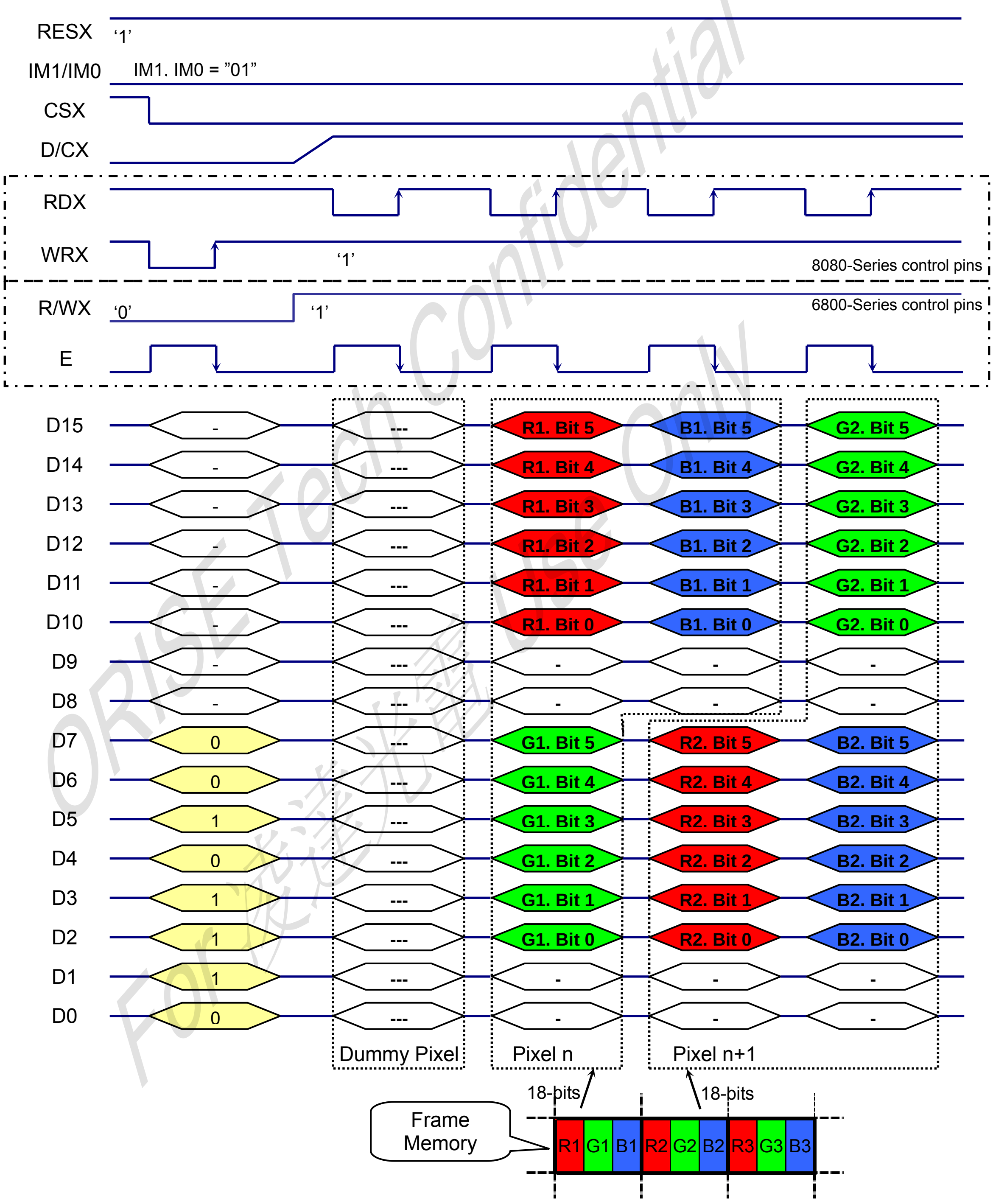
Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

7.3.2.2. Parallel 16-Bits Bus Interface for RAM Data Read (IM1, IM0= “01”)

There are 2 pixel (6 sub-pixels) per 3 bytes (RGB 6-6-6-bits output)



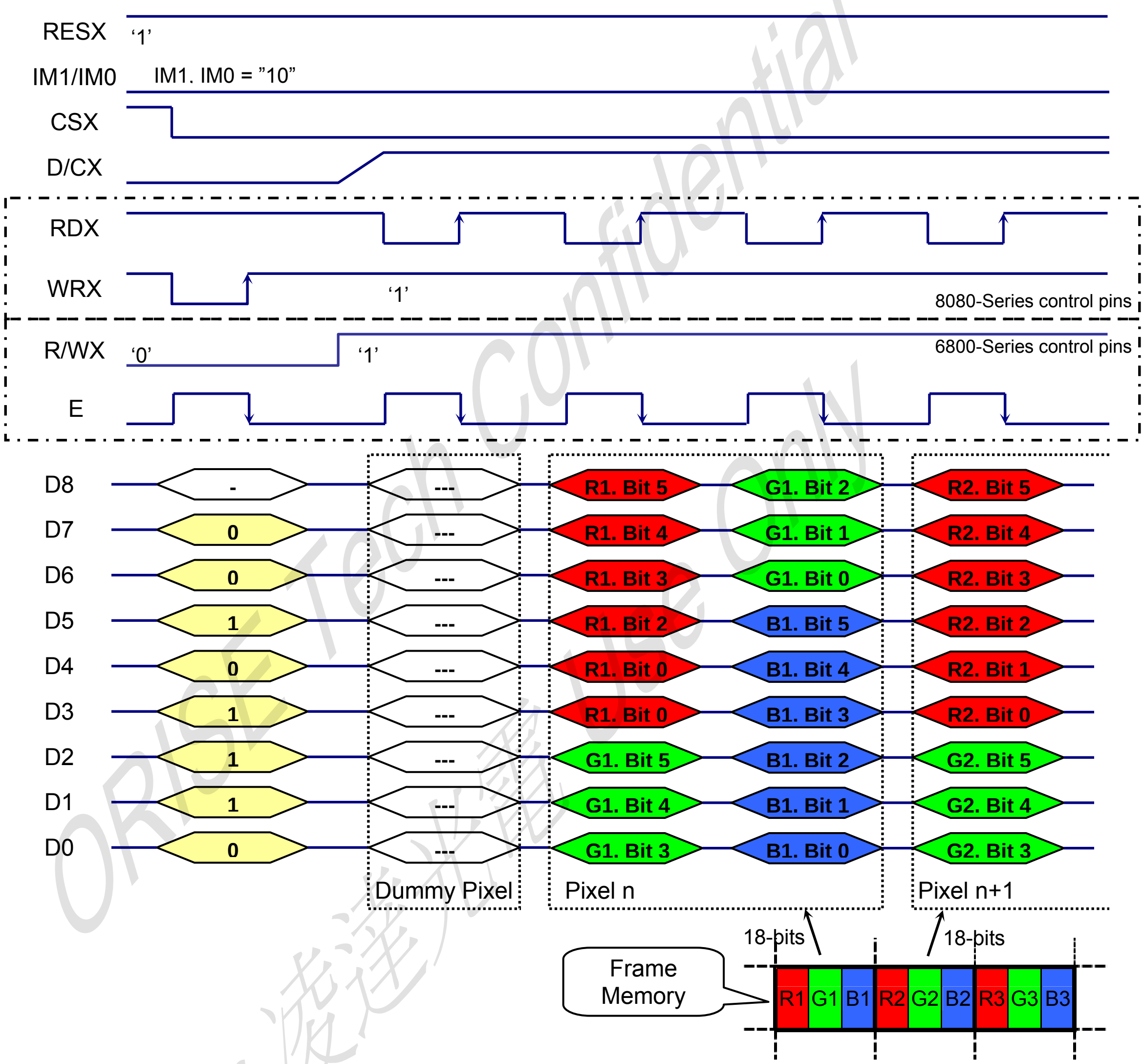
Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. ‘-‘ = Don't care - Can be set to VDDI or DGND level

7.3.2.3. Parallel 9-Bits Bus Interface for RAM Data Read (IM1, IM0= "10")

There are 1 pixel (3 sub-pixels) per 2 bytes (RGB 6-6-6-bits output)



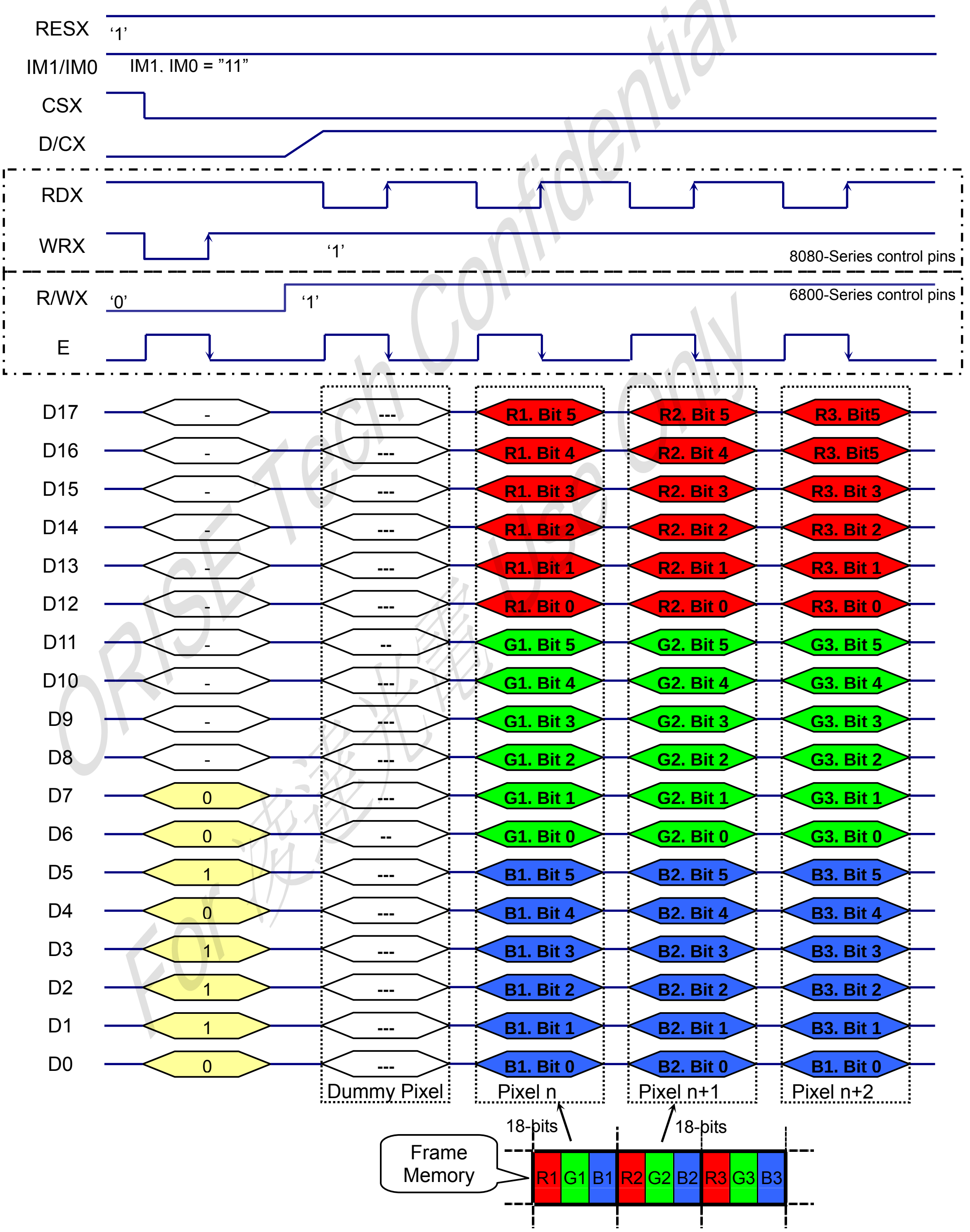
Note1. The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

7.3.2.4. Parallel 18-Bits Bus Interface for RAM Data Read (IM1, IM0= "11")

There are 1 pixel (3 sub-pixels) per 1 bytes (RGB 6-6-6-bits output)



Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

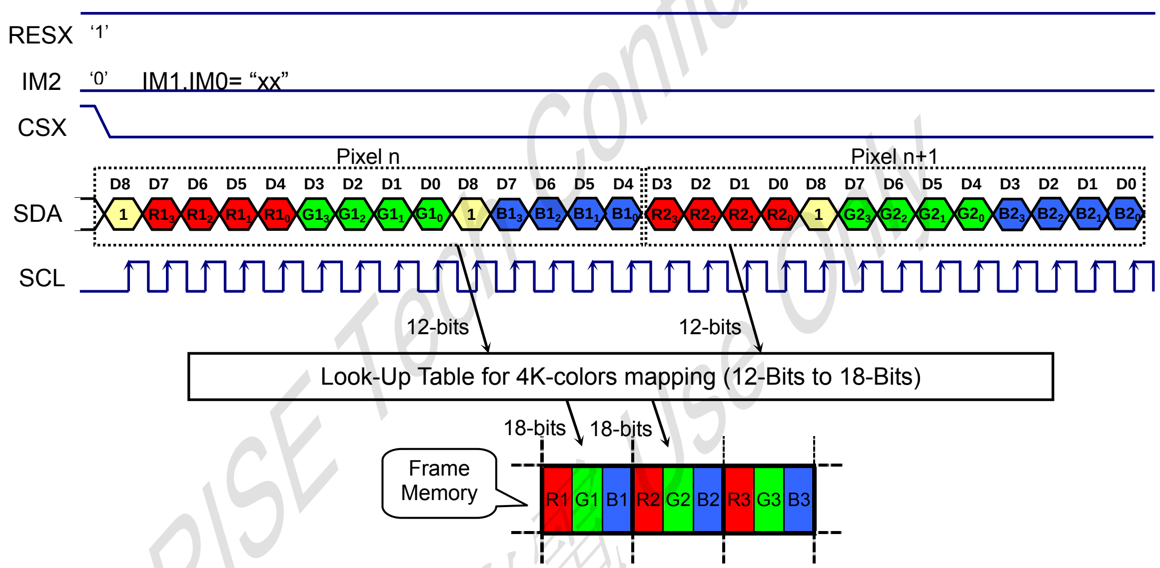
Note 3. '-' = Don't care - Can be set to VDDI or DGND level

7.3.3. Serial Interface (IM2 = '0')

Different display data formats are available for three colors depth supported by the LCM listed below.

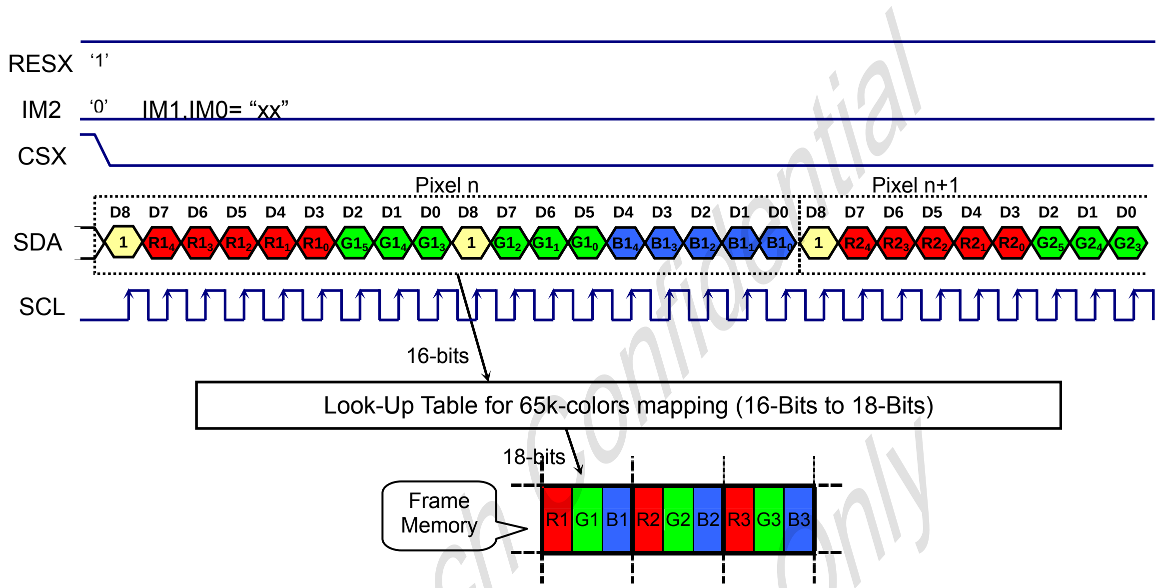
- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

7.3.3.1. Write data for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"



Note 1. pixel data with the 12-bits color depth information
Note 2. The most significant bits are: Rx_3, Gx_3 and Bx_3
Note 3. The least significant bits are: Rx_0, Gx_0 and Bx_0
Note 4. '-' = Don't care - Can be set to VDDI or DGND level

7.3.3.2. Write data for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"



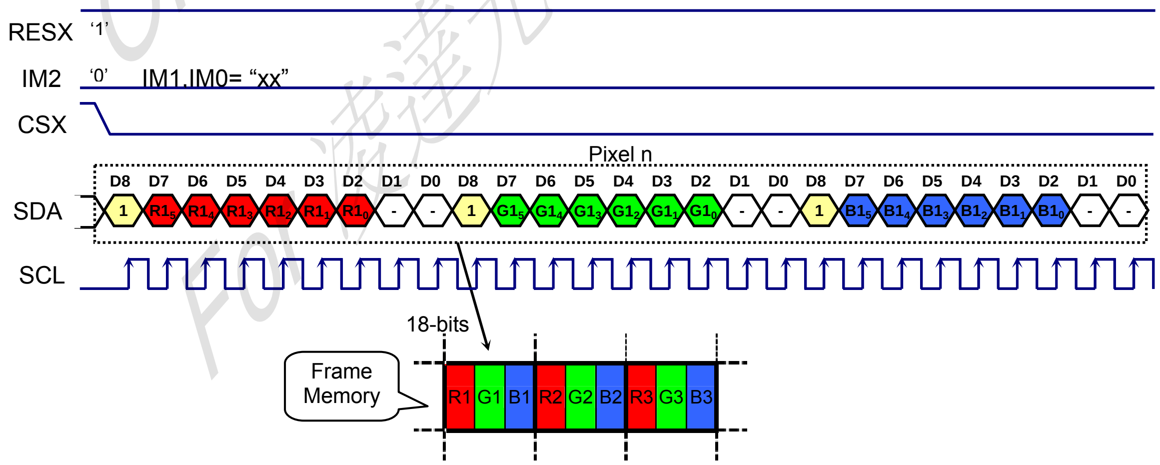
Note 1. pixel data with the 16-bits color depth information

Note 2. The most significant bits are: Rx_4, Gx_5 and Bx_4

Note 3. The least significant bits are: Rx_0, Gx_0 and Bx_0

Note 4. '-' = Don't care - Can be set to VDDI or DGND level

7.3.3.3. Write data for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"



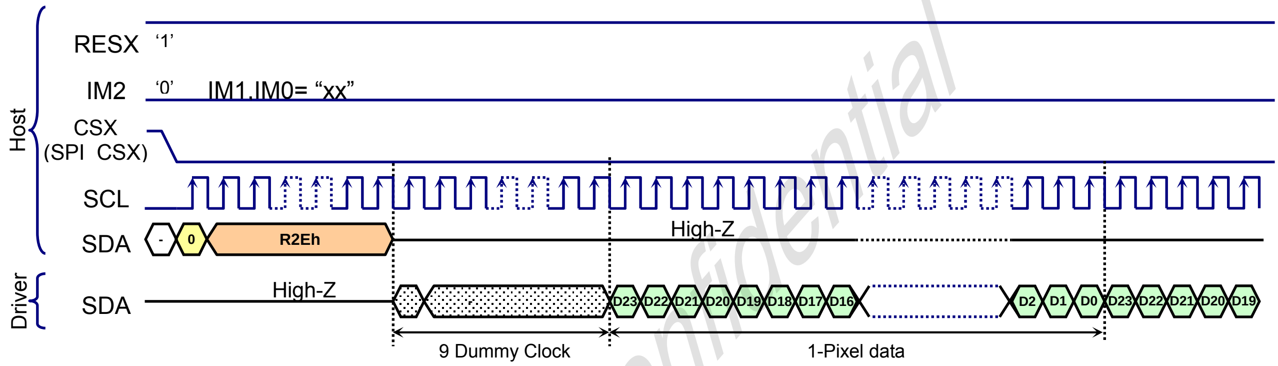
Note 1. pixel data with the 18-bits color depth information

Note 2. The most significant bits are: Rx_5, Gx_5 and Bx_5

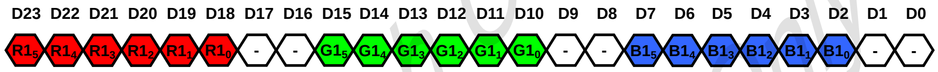
Note 3. The least significant bits are: Rx_0, Gx_0 and Bx_0

Note 4. '-' = Don't care - Can be set to VDDI or DGND level

7.3.3.4. Read data for Serial Interface (RGB 6-6-6-bits output)



Read Data format as below



Note: '-' = Don't care - Can be set to VDDI or DGND level

7.4. RGB interface

7.4.1. General Description

The module uses 6, 16 and 18-bits parallel RGB interface which includes: VS, HS, DE, PCLK, D[17:0]. The interface is activated after Power On sequence.

Pixel clock (PCLK) is running all the time without stoping and it is used to entering VS, HS, DE and D[17:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative ('0', low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative ('0', low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received a RGB information that should be transferred on the display. This is a positive ('1', high) active and its state is read to the display module by a rising edge of the PCLK signal.

D[17:0] (18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE='1' and there is a rising edge of PCLK). D[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the following figure.

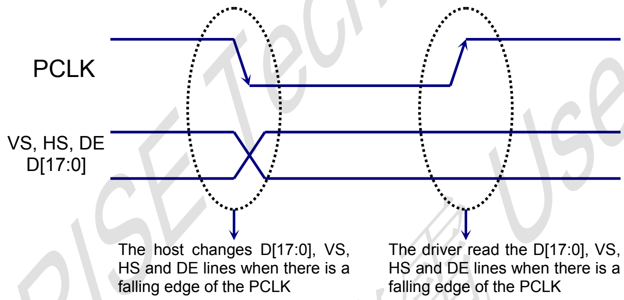


Fig. 7.4.1 PCLK cycle

Note: PCLK is an unsynchronized signal (It can be stopped).

7.4.2. General Timing Diagram

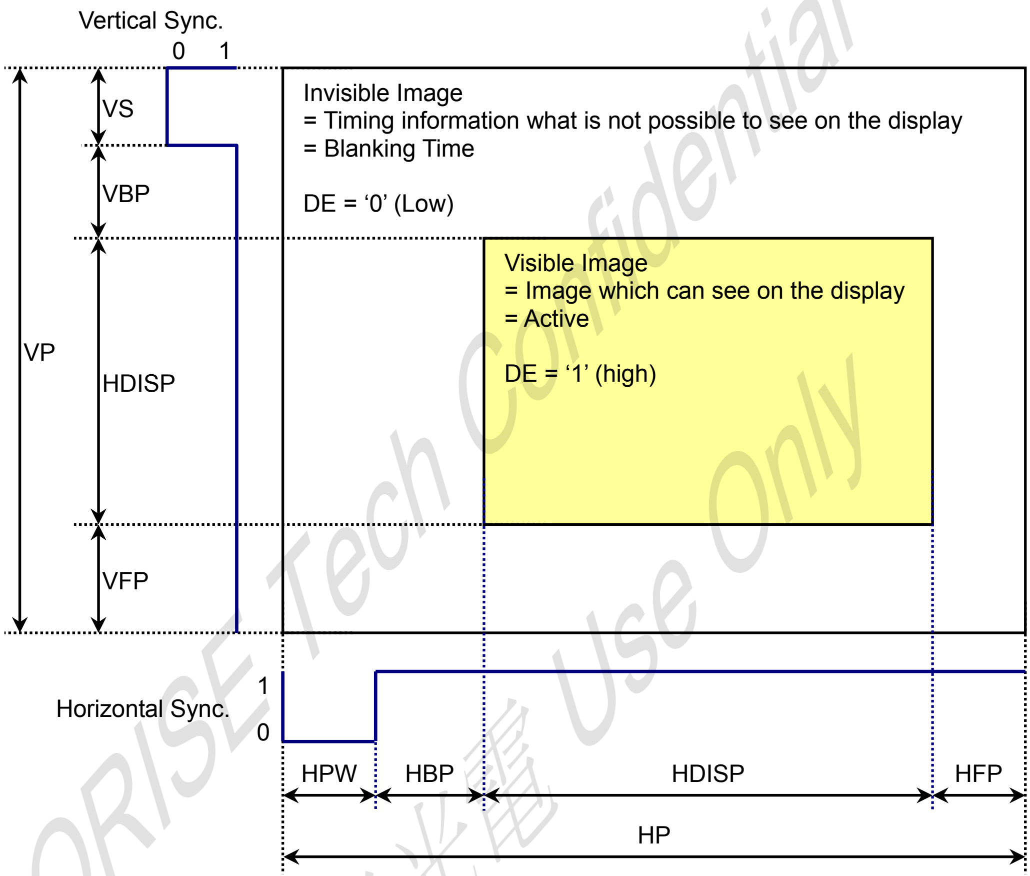


Fig. 7.4.2 RGB General Timing diagram

The image information must be correct on the display, when the timings are in range on the interface.

However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.

7.4.3. Updating Order on Display Active Area (Normal Display Mode On + Sleep Out)

There is defined different kind of updating orders for display. These updating orders are controlled by H/W (SMX, SMY) and S/W (MX, MY,) bits.

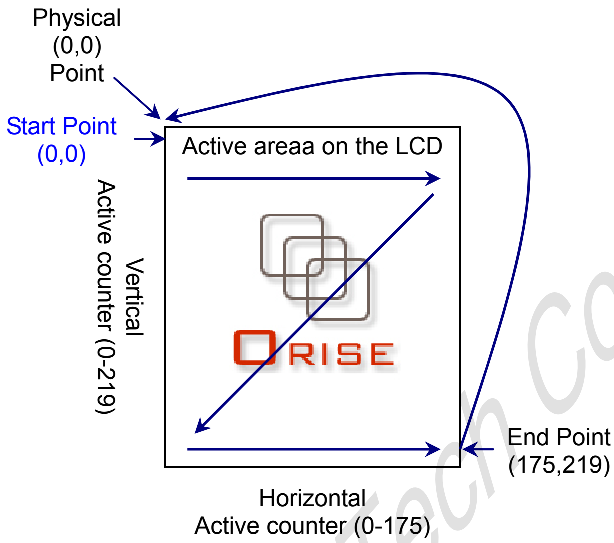


Fig. 7.4.3.1 Updating order when MADCTL's MX='0' and MY = '0'

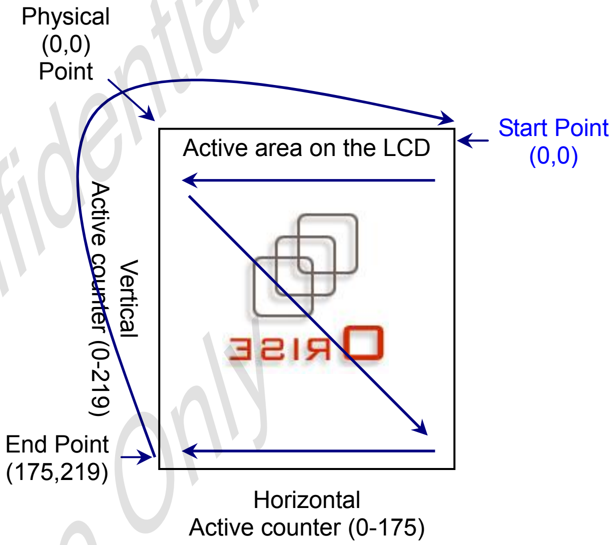


Fig. 7.4.3.2 Updating order when MADCTL's MX='1' and MY = '0'

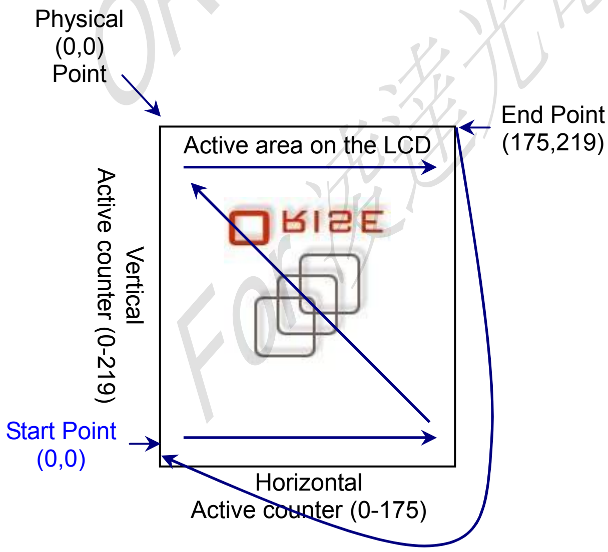


Fig. 7.4.3.3 Updating order when MADCTL's MX='0' and MY = '1'

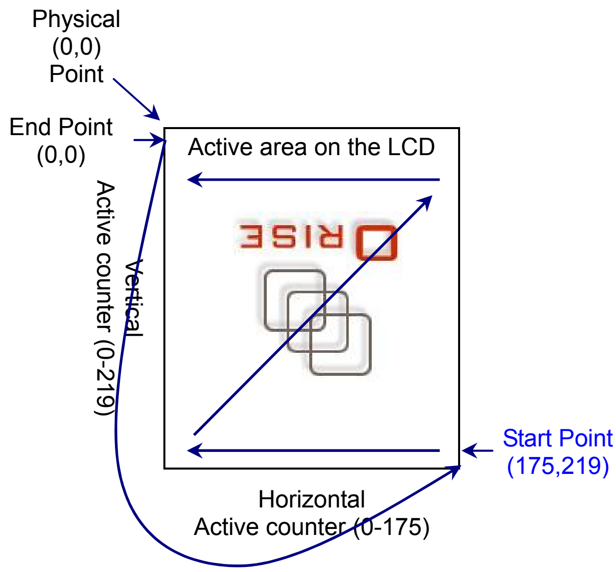


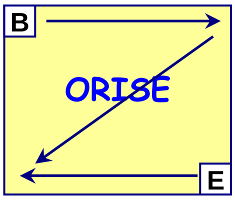
Fig. 7.4.3.4 Updating order when MADCTL's MX='1' and MY = '1'

Table 7.4.3.1 Rules for Updating Order

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Signal Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter is larger than 127 and the Vertical counter is larger than 159	Return to 0	Return to 0

Note 1. Pixel order is RGB on the display.

Note 2. Data streaming direction from the host to the display is described in the following figure.



Data Stream from RGB I/F is like in this figure

Fig. 7.4.3.5 Data streaming order from RGB I/F

7.4.4. RGB Interface Bus Width set

All 4-kinds of bus width can be available during RGB interface mode (selected by COLMOD (3Ah) command for 8-bits, 16-bits and 18-bits data width)

Table 7.4.4.1 RGB interface Bus Width Set Table

VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
0101	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bits data
0110	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bits data
VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
1110	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bits data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note 1: When VIPF[3:0]="1110", 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 2: Only VIPF[3:0]= "0101","0110" and "1110" are valid on RGB I/F, Others are invalid.

Note 3. 'x' Don't care, but need to set VDDI or DGND level.

7.4.5. RGB Interface Mode Set

Table 7.4.5.1 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	VS	HS	Video Data bus D[17:0]	Register for Blanking Porch setting	Reference clock for Display
RGB Mode 1	Used	Used	Used	Used	Used	Not Used	Internal Oscillator
RGB Mode 2	Used	Used	Used	Used	Used	Used	Internal Oscillator

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

In RGB Mode 1 (RCM1, RCM0 = "10"), writing data to frame memory is done by PCLK and Video Data Bus (D[17:0]), when DE is high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to SPFD54126B.

In RGB Mode 2 (RCM1, RCM0 = "11"), blanking porch setting of VS and HS signals are defined by RGBBPCTR (B5h) command. When DE pin is high, valid data is directly stored to frame memory.

7.4.6. RGB Interface Timing Diagram

7.4.6.1. General Timings for RGB I/F

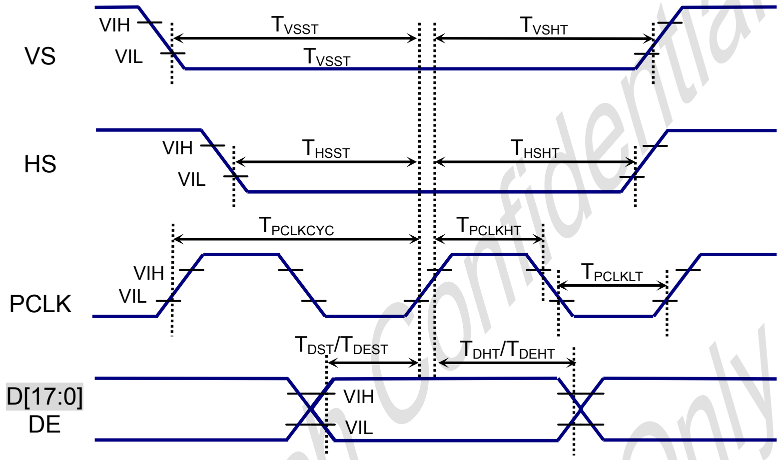


Fig. 7.4.6.1.1 General Timing for RGB I/F

Table 7.4.6.1.1 General Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Pixel low pulse width	T_{PCLKLT}		15			
Pixel high pulse width	T_{PCLKHT}		15			
Vertical Sync. set-up time	T_{VSST}		15			ns
Vertical Sync. hold time	T_{VSSHT}		15			ns
Horizontal Sync. set-up time	T_{HSST}		15			ns
Horizontal Sync. hold time	T_{VSSHT}		15			ns
Data Enable set-up time	T_{DEST}		15			
Data Enable hold time	T_{DEHT}		15			
Data set-up time	T_{DST}		15			
Data hold time	T_{DHT}		15			

Note 1: VDDI=1.6 to 3.6V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Note 3. Data lines can be set to “High” or “Low” during blanking time – Don’t care.

Note 4. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

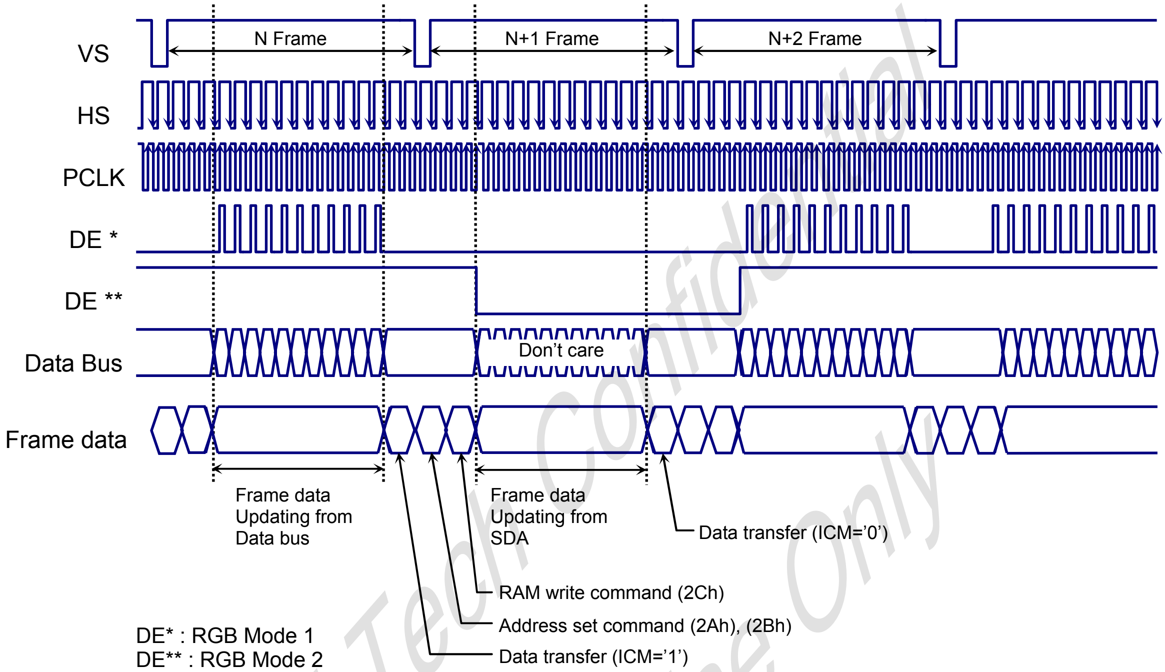


Fig. 7.4.6.1.2 RAM Access via SPI Interface in RGB Mode

7.4.6.2. RGB Interface Mode 1 Timing Diagram

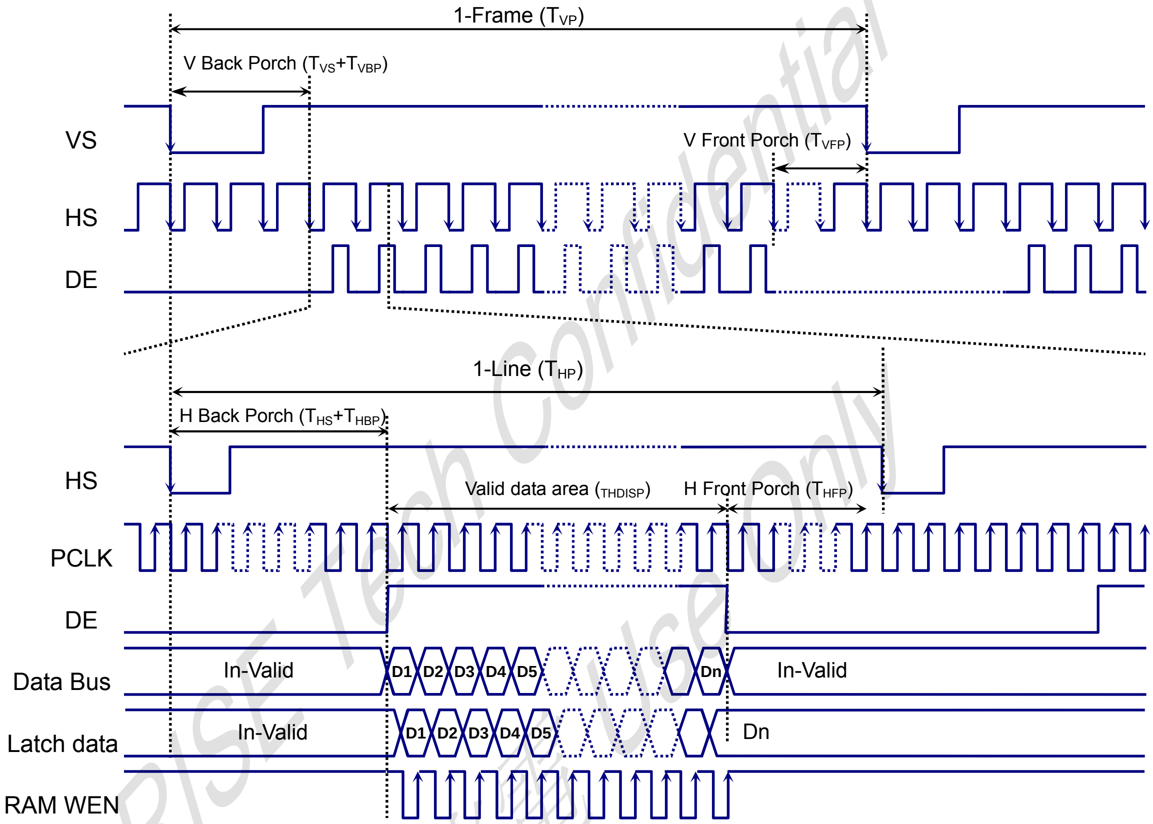
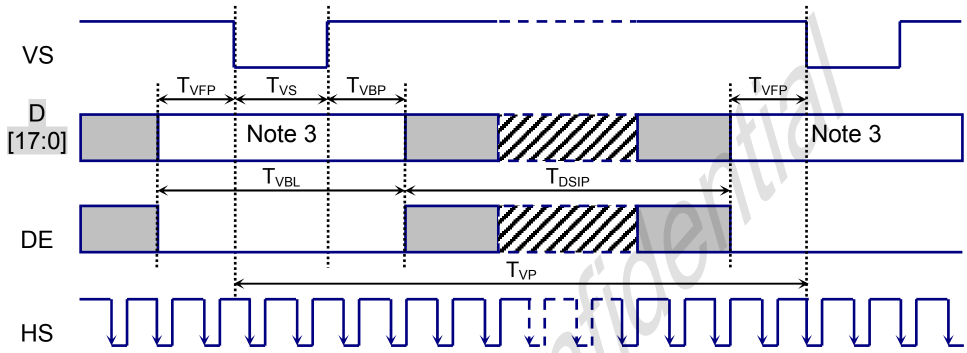


Fig. 7.4.6.2.1 RGB Mode 1 Timing Diagram

Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F

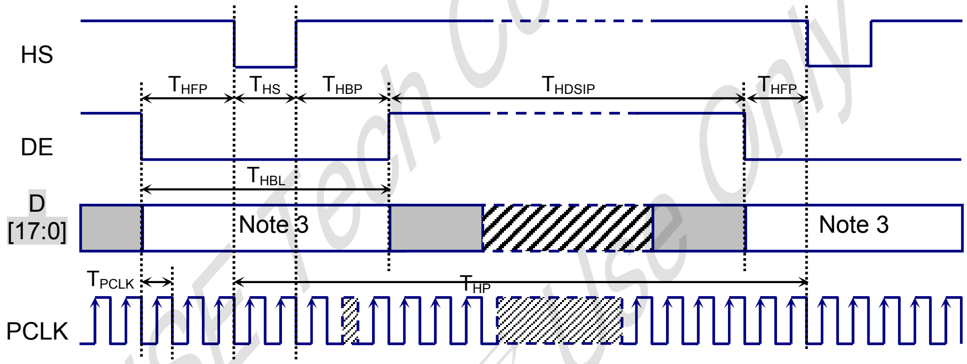


Fig. 7.4.6.2.2 Vertical and Horizontal timing for RGB I/F

Table 7.4.6.2.1 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	GM="00"	226		230	HS
		GM="01"	182		186	HS
		GM="11"	179		183	
Vertical low pulse width	T_{VS}		2		4	HS
Vertical front porch	T_{VFP}		2		4	HS
Vertical back porch	T_{VBP}		2		4	HS
Vertical data start line		$T_{VS} + T_{VBP}$	4		8	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	6		12	HS
Vertical active area	T_{VDISP}	GM="00"		220		HS
		GM="01"		176		
		GM="11"		132		
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}		208		512	PCLK
Horizontal low pulse width	T_{HS}		2		256	PCLK
Horizontal front porch	T_{HFP}		2		256	PCLK
Horizontal back porch	T_{HBP}		2		256	PCLK
Horizontal data start point		$T_{HS} + T_{HBP}$	30		256	PCLK
		$ff_{HS} + f_{HBP}$	1.0			µs
Horizontal blanking period	T_{HBL}		32		256	PCLK
Horizontal active area	T_{HDISP}			176		PCLK
Pixel clock cycle	$T_{PCLKCYC}$	GM="00"	100		355	ns
	$f_{PCLKCYC}$	TVRR=65Hz	2.82		10	MHz
	$T_{PCLKCYC}$	GM="01"	100		440	ns
	$f_{PCLKCYC}$	TVRR=65Hz	2.27		10	MHz
	$T_{PCLKCYC}$	GM="10"	100		581	ns
	$f_{PCLKCYC}$	TVRR=65Hz	1.72		10	MHz

7.4.6.3. RGB Interface Mode 2 Timing Diagram

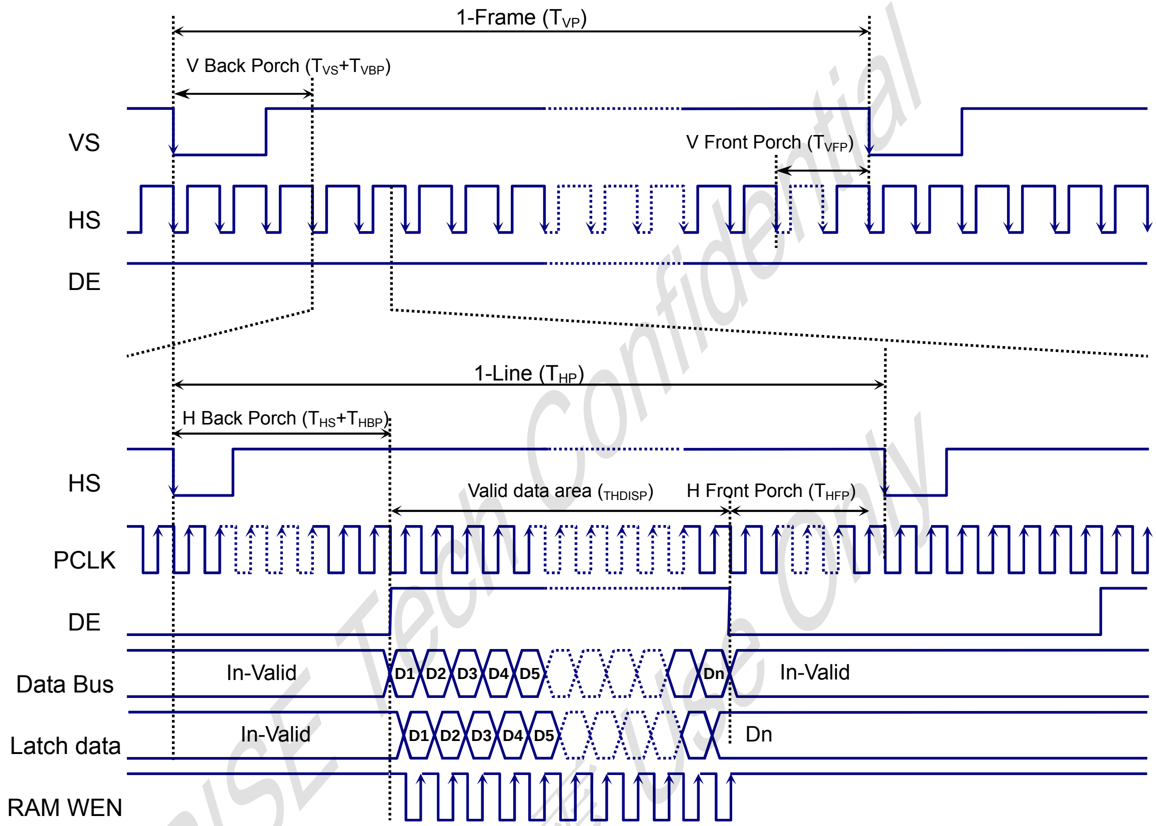


Fig. 7.4.6.3.1 RGB Mode 2 Timing Diagram

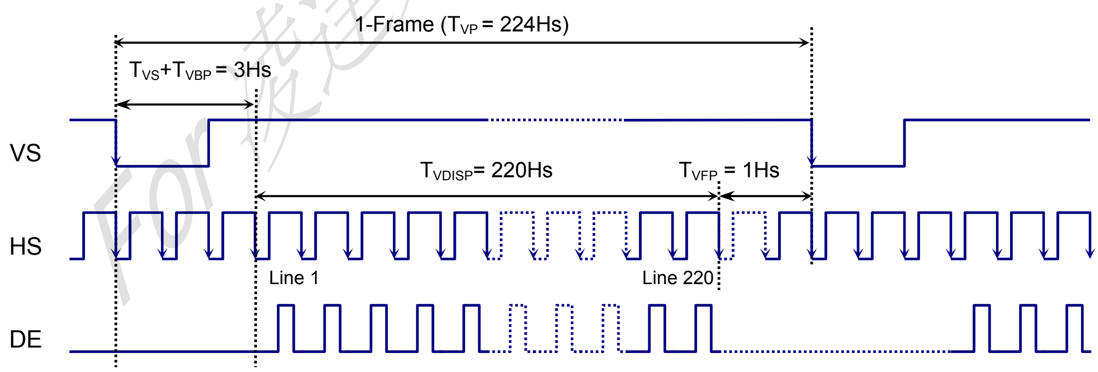


Fig. 7.4.6.3.2 RGB Mode 2 Vertical Timing Diagram

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

-176xRGBx220

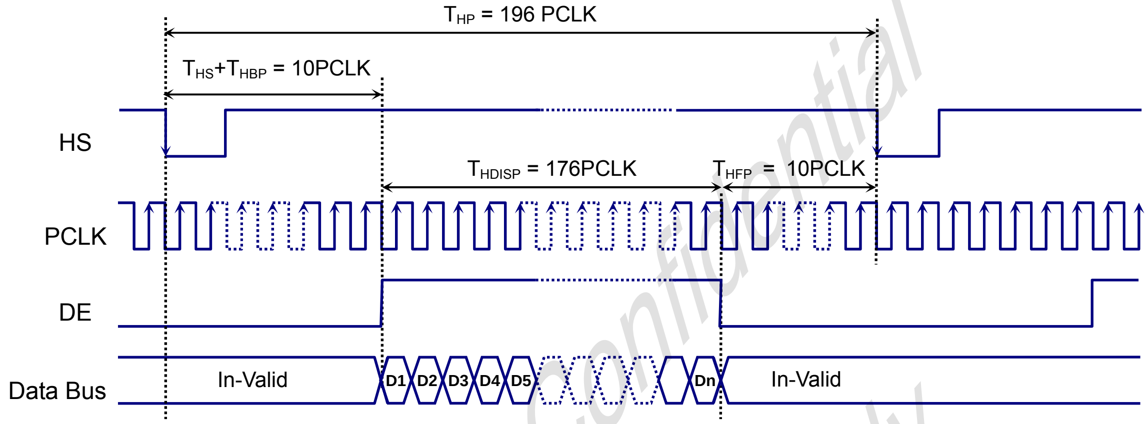


Fig. 7.4.6.3.3 RGB Mode 2 Horizontal Timing Diagram

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

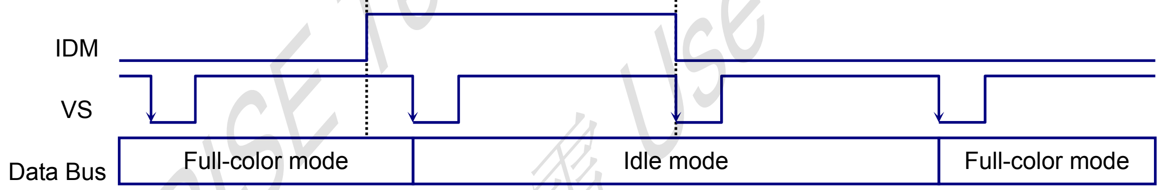
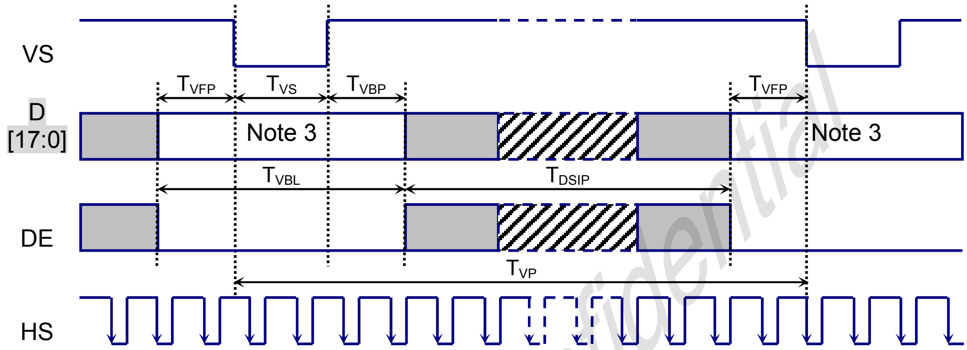


Fig. 7.4.6.3.4 RGB Mode 2 Idle mode Timing Diagram

Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F

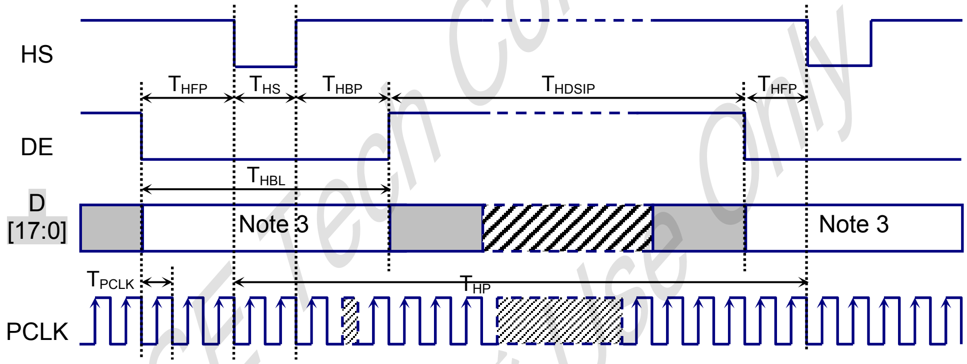


Fig. 7.4.6.3.5 Vertical and Horizontal timing for RGB I/F

Table 7.4.6.3.1 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	GM="00"	223	224		HS
		GM="01"	176	180		HS
		GM="11"	135	136		
Vertical low pulse width	T_{VS}		1		4	HS
Vertical front porch	T_{VFP}		1	1	1023	HS
Vertical back porch	T_{VBP}		1		1022	HS
Vertical data start line		$T_{VS} + T_{VBP}$	2	3	1023	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	3	4	1023	HS
Vertical active area	T_{VDISP}	GM="00"		220		HS
		GM="01"		176		
		GM="11"		132		HS
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}		176	196	511	PCLK
Horizontal low pulse width	T_{HS}		1		63	PCLK
Horizontal front porch	T_{HFP}		1	10	63	PCLK
Horizontal back porch	T_{HBP}		1		62	PCLK
Horizontal data start point		$T_{HS} + T_{HBP}$	2	10	63	PCLK
		$ff_{HS} + f_{HBP}$	TBD			µs
Horizontal blanking period	T_{HBL}	$T_{HS} + T_{HBP} + T_{HFP}$	3	20	256	PCLK
Horizontal active area	T_{HDISP}			176		PCLK
Pixel clock cycle	$T_{PCLKCYC}$	GM="00"	100	380	418	Ns
	$f_{PCLKCYC}$	TVRR=65Hz	2.40	2.63	10	MHz
	$T_{PCLKCYC}$	GM="01"	100	472	520	Ns
	$f_{PCLKCYC}$	TVRR=65Hz	1.92	2.12	10	MHz
	$T_{PCLKCYC}$	GM="10"	100	625	690	Ns
	$f_{PCLKCYC}$	TVRR=65Hz	1.45	1.60	10	MHz

Note 1. VDD1=1.6 to 3.6V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.

7.4.6.4. Power On Sequence on RGB Mode 2

The Driver operates power up and display ON by VDD, VDDI, SHUT, VS, HS, DE, PCLK on RGB mode 2 as show as following figure.

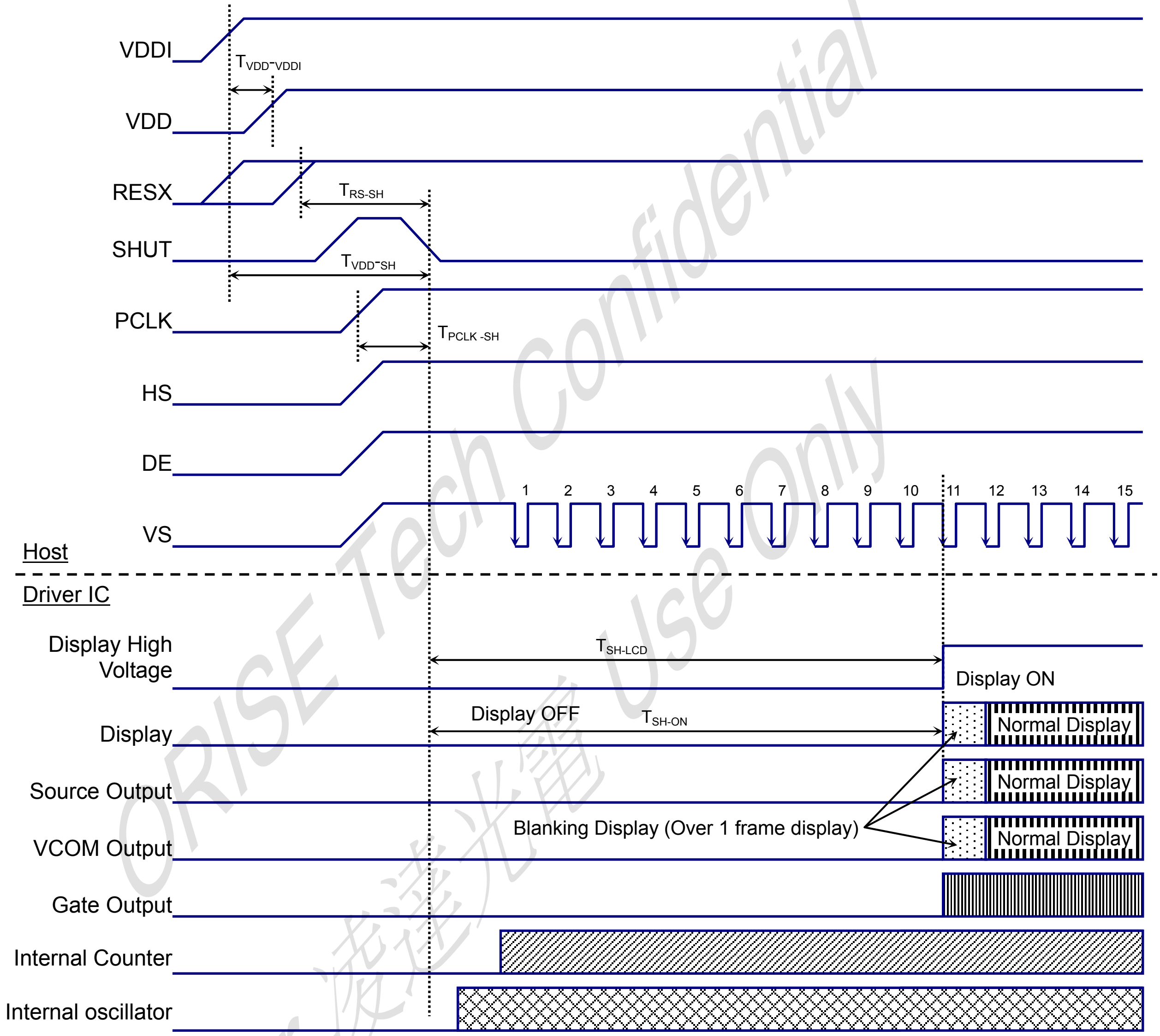


Fig. 7.4.6.4.1 Power On Sequence on RGB Mode 2

Table 7.4.6.4.1 Power ON AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	$T_{VDDI-VDD}$	0			ns	Note1
VDDI/VDD on to falling edge of SHUT	T_{VDD-SH}	1			ms	
RESX to falling of SHUT	T_{RS-SH}	10			us	
Signals input to falling edge of SHUT *	T_{CLK-SH}	1			PCLK	Note2
Falling edge of SHUT to LCD power ON	T_{SH-LCD}			120	ms	
Falling edge of SHUT to Display start	T_{SH-ON}		10		VS	

Note 1: $T_{VDDI-VDD}$ can be <=0ns, >0ns. In any case, VDDI and VDD power up sequence should not have any impact on the driver / display functionalities / performance.

Note 2: Signals mean VS, HS, DE and PCLK signal.

Note 3: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

7.4.6.5. Power OFF Sequence on RGB Mode 2

The Driver operates power off and display OFF by VDD, VDDI, SHUT, VS, HS and DE on RGB mode 2 as show as following figure.

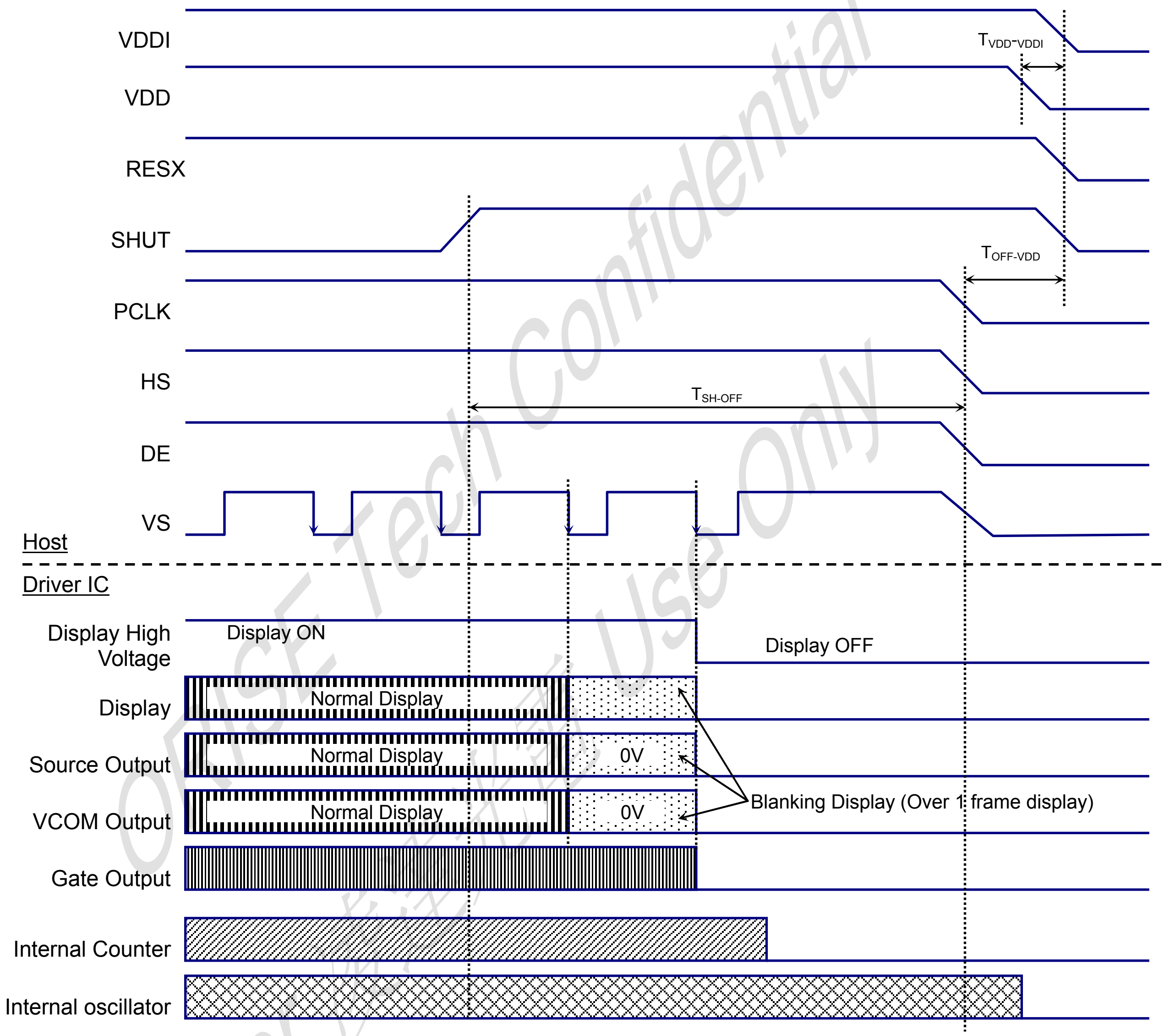


Fig. 7.4.6.5.1 Power OFF Sequence on RGB Mode 2

Table 7.4.6.5.1 Power OFF AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	$T_{VDDI-VDD}$	0			ns	Note1
Signals input to VDDI/VDD off	$T_{off-VDD}$	1			us	Note2
Rising edge of SHUT to Display off	T_{SH-OFF}	2			VS	

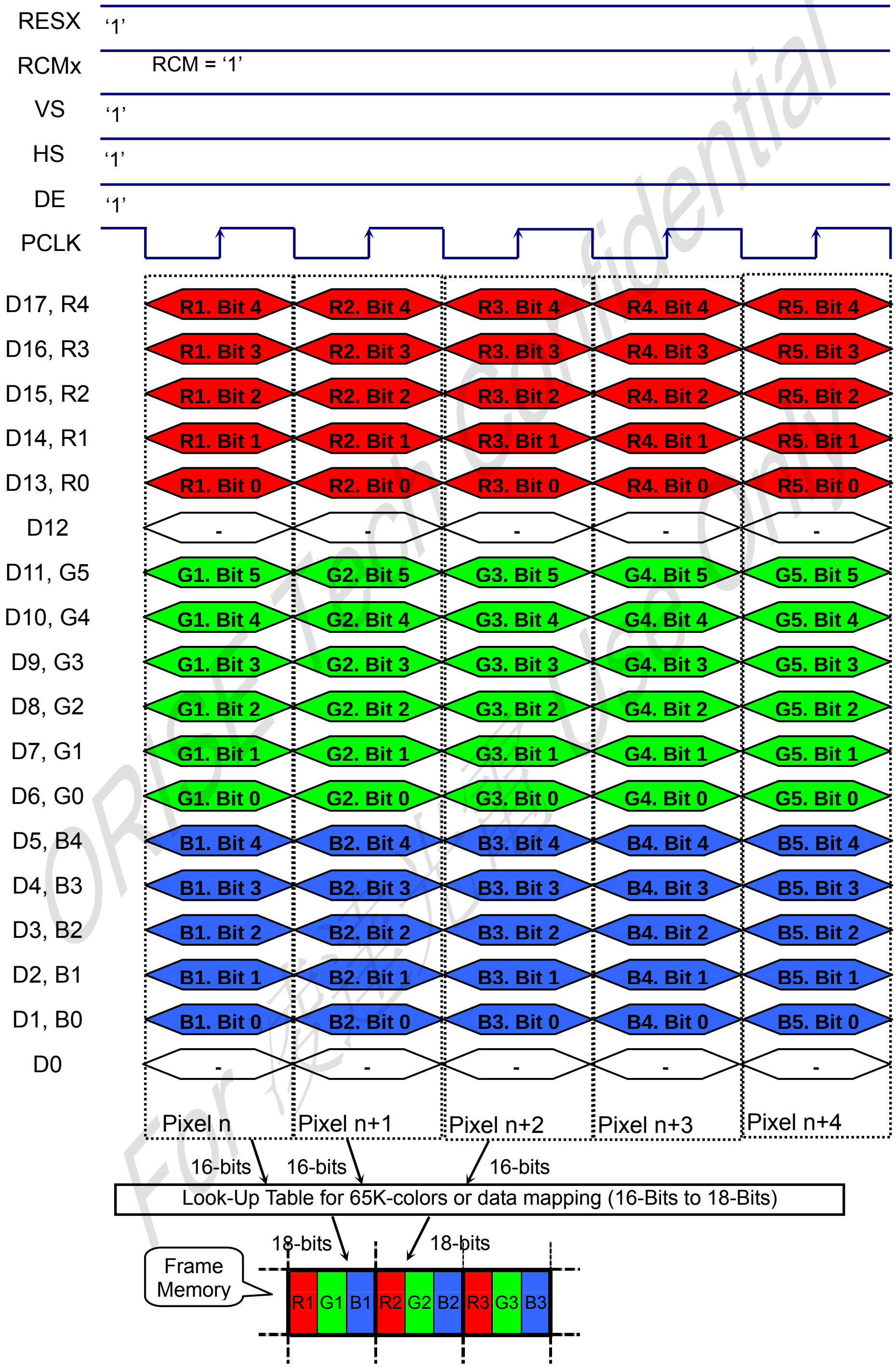
Note 1: $T_{VDDI-VDD}$ can be <=0ns, >0ns. In any case, VDDI and VDD power up sequence should not have any impact on the driver / display functionalities / performance.

Note 2: Signals mean VS, HS, DE and PCLK signal.

Note 3: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

7.4.7. RGB Data Color Coding

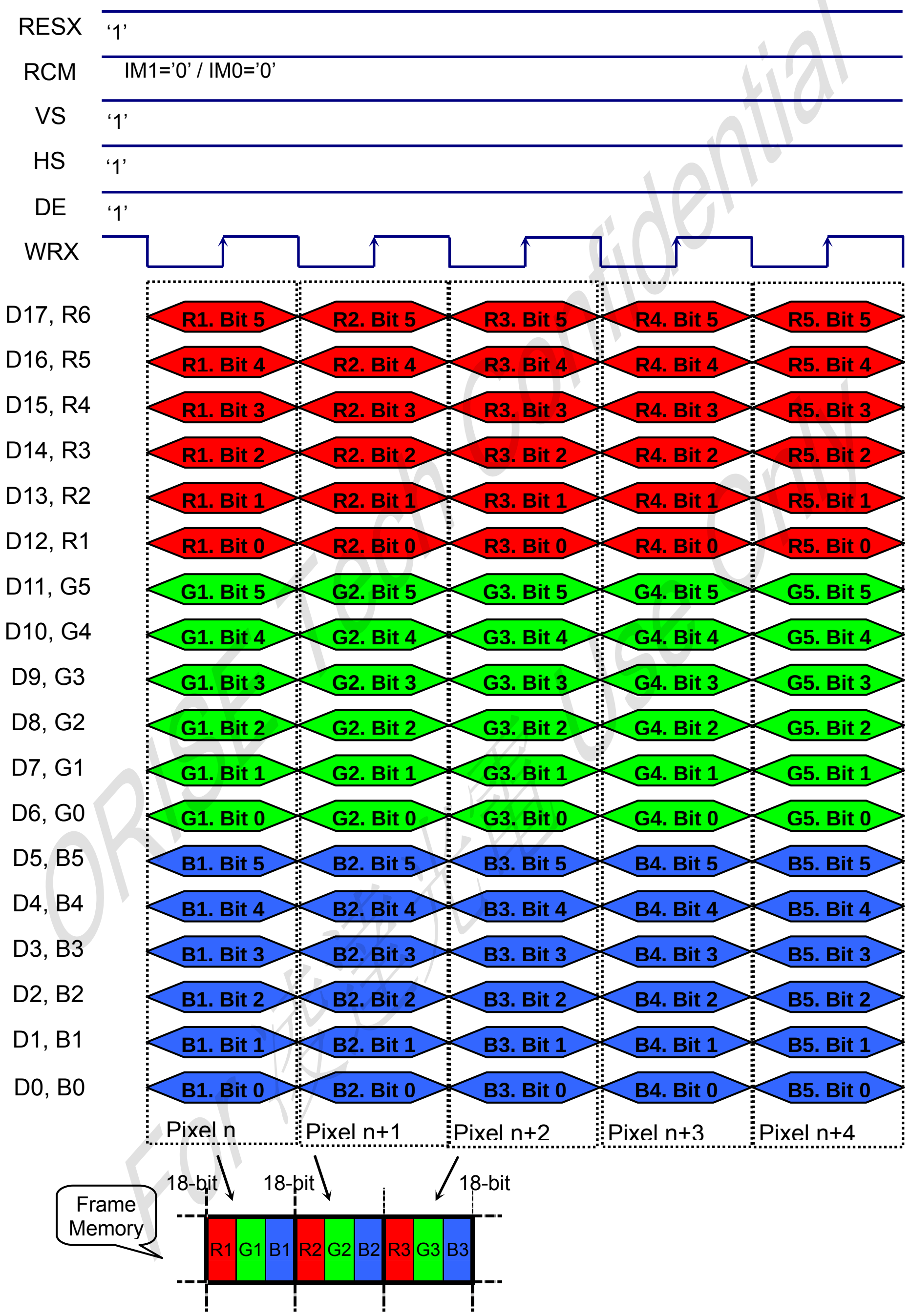
7.4.7.1. 16-bits/pixel Colour Order on the RGB Interface



Note 1: The data order is as follows, MSB=D23, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Note 2. '-' Don't care, but need set to VDDI or DGND level.

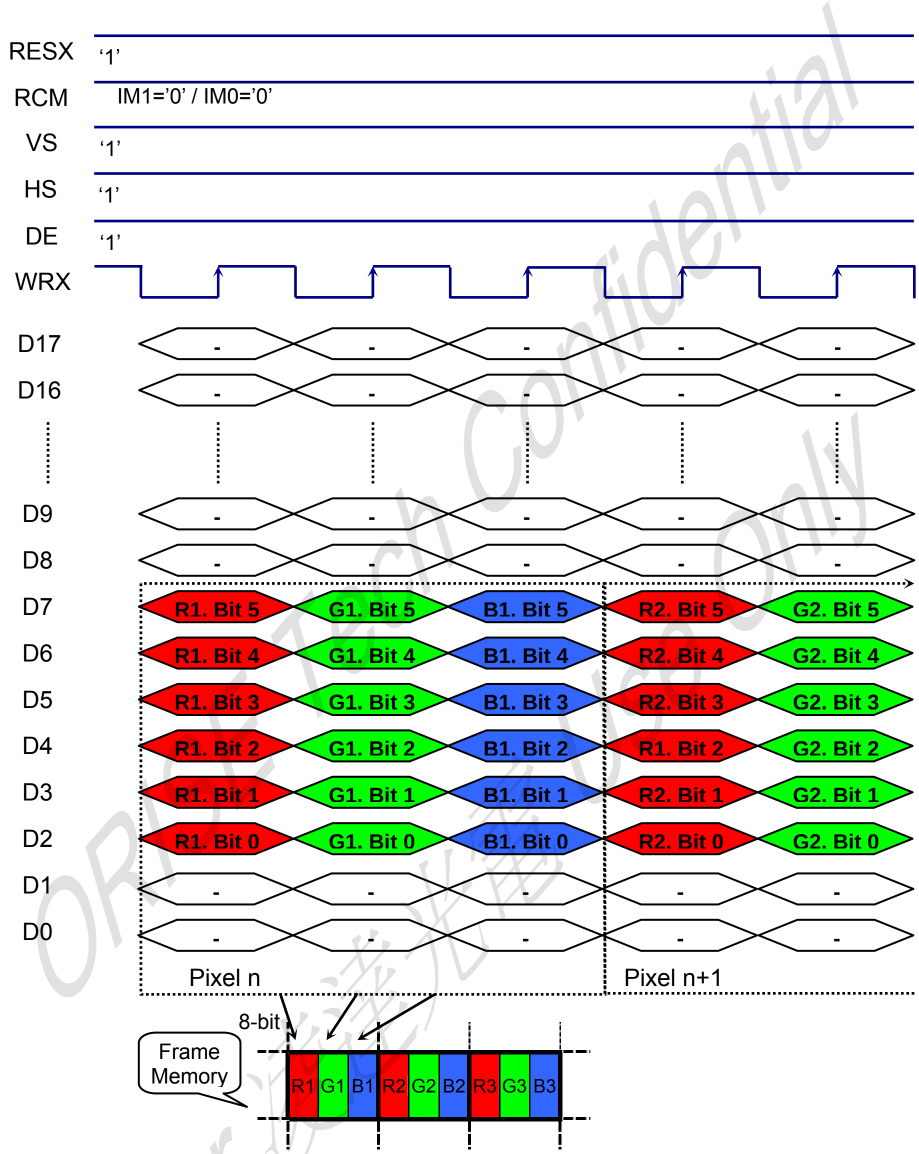
7.4.7.2. 18-bits/pixel Colour Order on the RGB Interface



Note 1: The data order is as follows, MSB=D23, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.

Note 2. '-' Don't care, but need set to VDDI or DGND level.

7.4.7.3. 6-bits/pixel Colour Order on the RGB Interface



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.
Note 2. '-' Don't care, but need set to VDDI or DGND level.

7.5. Display Data RAM

7.5.1. Configuration

The display module has an integrated 176x220x18-bit graphic type static RAM. This 696,960-bits memory allows to store on-chip a 176xRGBx220 image with an 18-bpp resolution (262K-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and interface Read or Write to the same location of the Frame Memory.

Display Data RAM Organization (GM='00')

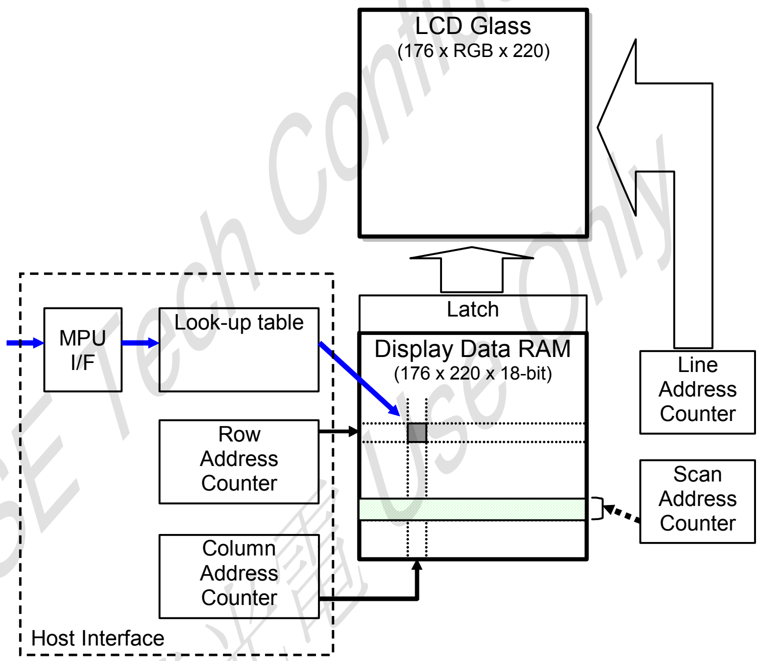


Fig. 7.5.1.1 Display Date RAM Organization

7.5.2. Memory to Display Address Mapping

7.5.2.1. When using 176RGB x 220 resolution (GM1, GM0 = “00”, SMX=SMY=SRGB=’0’)

			Pixel 1			Pixel 2			--------	Pixel 175			Pixel 176				
Gate Out	Source Out		S1	S2	S3	S4	S5	S6	--------	S523	S524	S525	S526	S527	S528		
			RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1		
	RA															SA	
	MY='0'	MY='1'														ML='0'	ML='1'
1	0	219	R0	G0	B0	R1	G1	B1	--------	R174	G174	B174	R175	G175	B175	0	219
2	1	218							--------							1	218
3	2	217							--------							2	217
4	3	216							--------							3	216
5	4	215							--------							4	215
6	5	214							--------							5	214
7	6	213							--------							6	213
8	7	212							--------							7	212
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
213	212	7							--------							212	7
214	213	6							--------							213	6
215	214	5							--------							214	5
216	215	4							--------							215	4
217	216	3							--------							216	3
218	217	2							--------							217	2
219	218	1							--------							218	1
220	219	0							--------							219	0
	CA	MX='0'	0			1			--------	174			175				
		MX='1'	175			174			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

MX =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

7.5.2.2. When using 176RGB x 176 resolution (GM1, GM0 = “01”, SMX=SMY=SRGB=’0’)

			Pixel 1			Pixel 2			--------	Pixel 175			Pixel 176				
Gate Out	**Source Out**		**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**--------**	**S523**	**S524**	**S525**	**S526**	**S527**	**S528**		
	RA		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=’0’	MY=’1’														ML=’0’	ML=’1’
1	0	175	R0	G0	B0	R1	G1	B1	--------	R118	G118	B118	R119	G119	B119	0	175
2	1	174							--------							1	174
3	2	173							--------							2	173
4	3	172							--------							3	172
5	4	171							--------							4	171
6	5	170							--------							5	170
7	6	169							--------							6	169
¦	¦	¦	¦	¦	¦	¦	¦	¦	¦	¦	¦	¦	¦	¦	¦	¦	¦
170	169	6							--------							169	6
171	170	5							--------							170	5
172	171	4							--------							171	4
173	172	3							--------							172	3
174	173	2							--------							173	2
175	174	1							--------							174	1
176	175	0							--------							175	0
	CA	MX=’0’	0			1			--------	174			175				
		MX=’1’	175			174			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

MX =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

7.5.2.3. When using 176RGB x 132 resolution (GM1, GM0 = “11”, SMX=SMY=SRGB=’0’)

			Pixel 1			Pixel 2			--------	Pixel 175			Pixel 176				
Gate Out	Source Out		S7	S8	S9	S10	S11	S12	--------	S523	S524	S525	S526	S527	S528		
	RA		RGB=0	RGB=1		RGB=0	RGB=1		RGB Order	RGB=0	RGB=1		RGB=0	RGB=1		SA	
	MY=’0’	MY=’1’														ML=’0’	ML=’1’
1	0	131	R0	G0	B0	R1	G1	B1	--------	R174	G174	B174	R175	G175	B175	0	131
2	1	130							--------							1	130
3	2	129							--------							2	129
4	3	128							--------							3	128
5	4	127							--------							4	127
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
128	127	4							--------							127	4
129	128	3							--------							128	3
130	129	2							--------							129	2
131	130	1							--------							130	1
132	131	0							--------							131	0
	CA	MX=’0’	0			1			--------	174			175				
		MX=’1’	175			174			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

MX =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

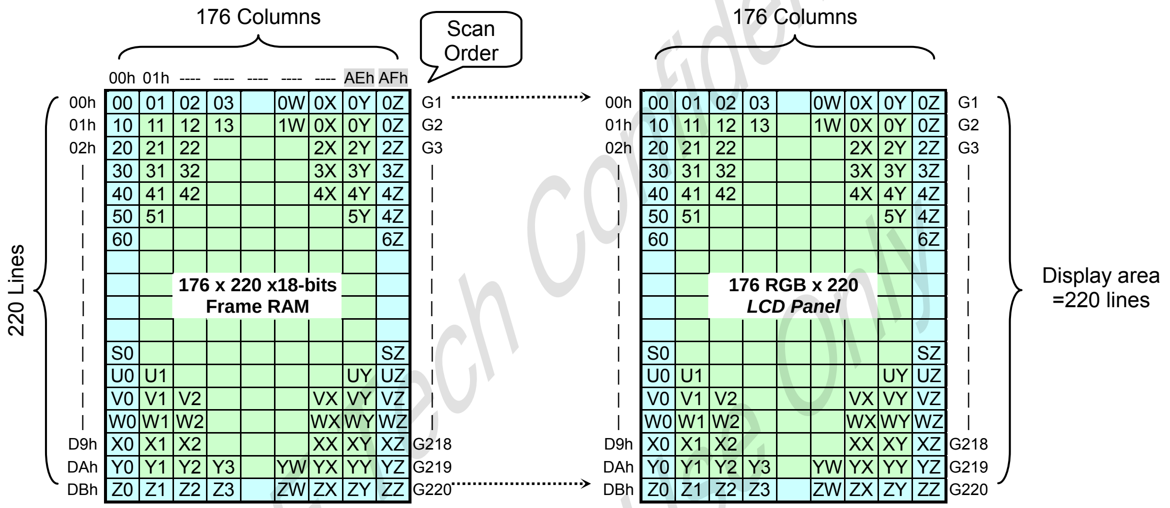
7.5.3. Normal Display On or Partial Mode On, Vertical Scroll Off

7.5.3.1. When using 176RGB x 220 resolution (GM1, GM0 = “00”)

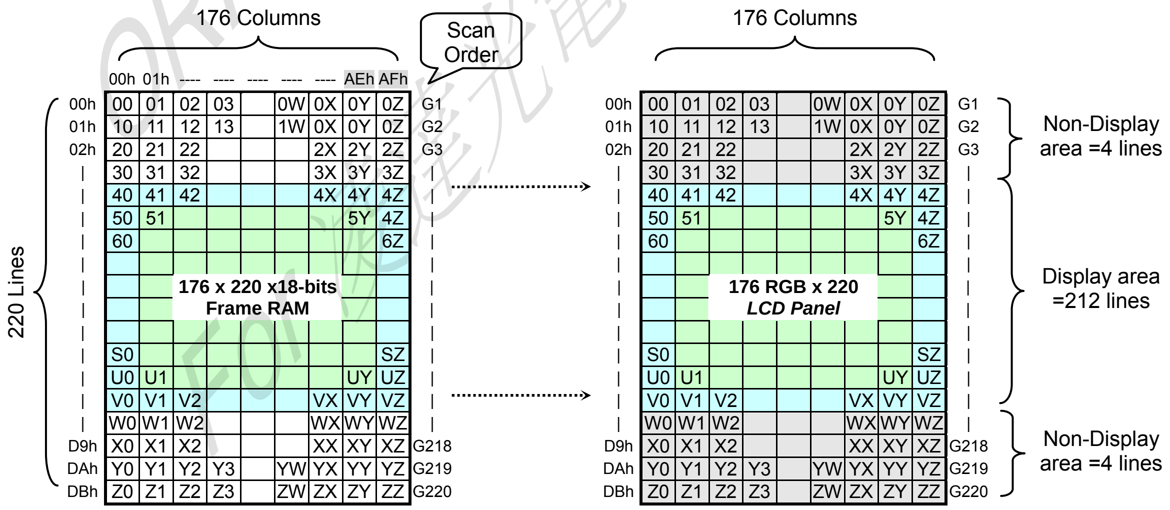
In this mode, content of the frame memory within an area where column pointer is 00h to AFh and page pointer is 00h to DBh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

(1) Example for Normal Display On (MX=MY=ML=’0’ ,SMX=SMY=’0’)



(2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=D7h, MX=MV=ML=’0’ ,SMX=SMY=’0’)

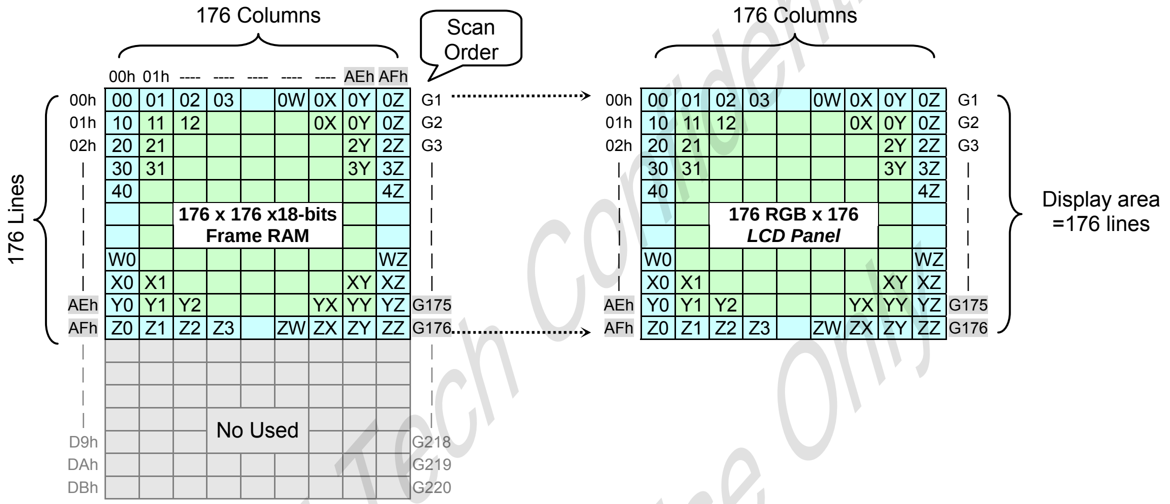


7.5.3.2. When using 176RGB x 176 resolution (GM1, GM0 = "01")

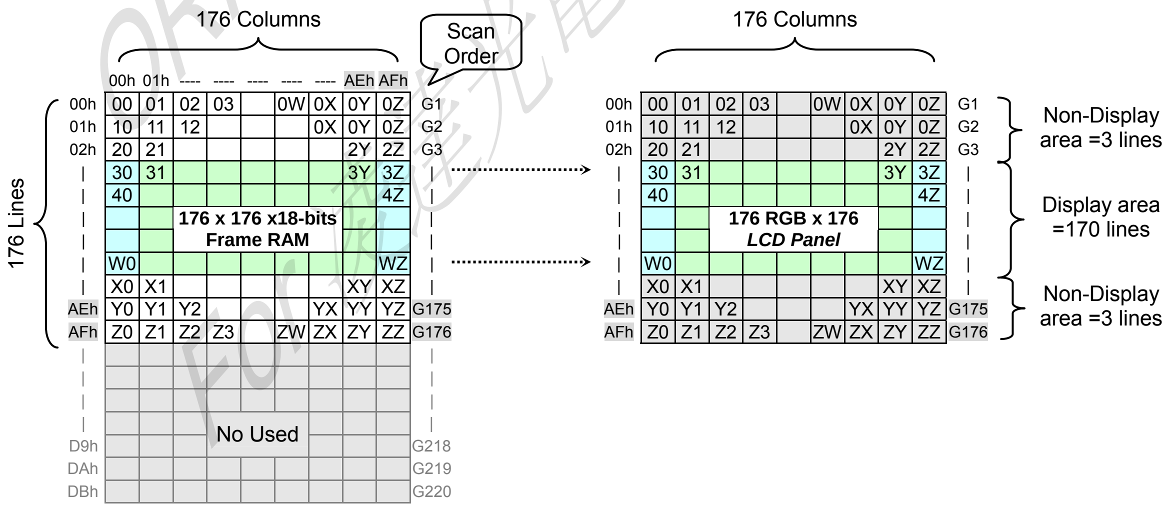
In this mode, contents of the frame memory within an area where column pointer is 00h to AFh and page pointer is 00h to AFh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

(1) Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



(2) Example for Partial Display On (PSL[7:0]=03h,PEL[7:0]=ACh, MX=MV=ML='0', SMX=SMY='0')

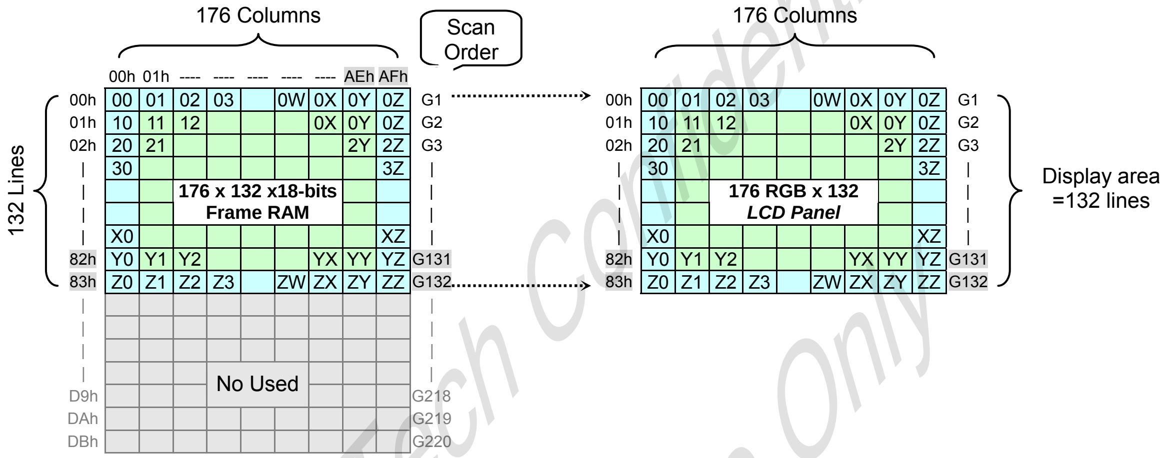


7.5.3.3. When using 176RGB x 132 resolution (GM1, GM0 = "11")

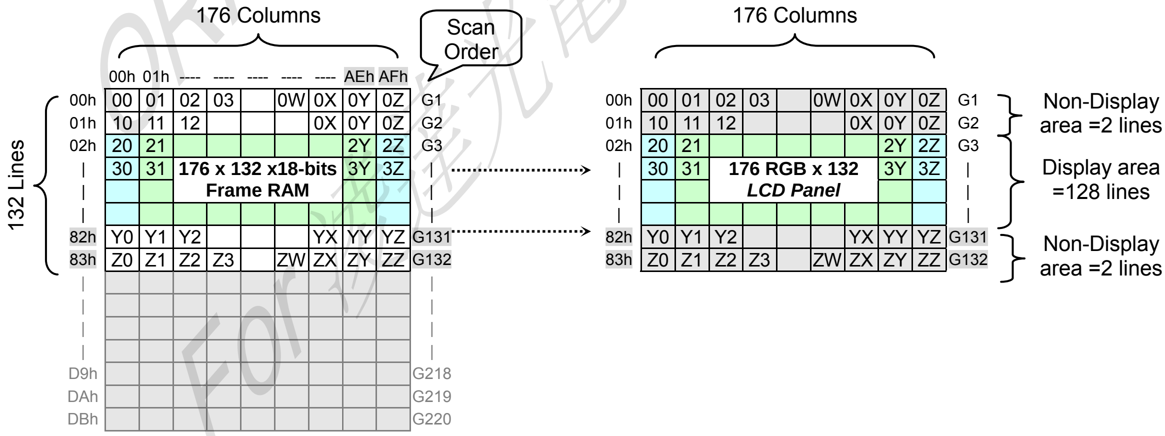
In this mode, contents of the frame memory within an area where column pointer is 00h to AFh and page pointer is 000h to 83h is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

(1) Example for Normal Display On (MX=MY=ML='0' ,SMX=SMY='0')



(2) Example for Partial Display On (PSL[7:0]=02h,PEL[7:0]=81h, MX=MV=ML='0' ,SMX=SMY='0')



7.5.4. Vertical Scroll Mode

There is vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

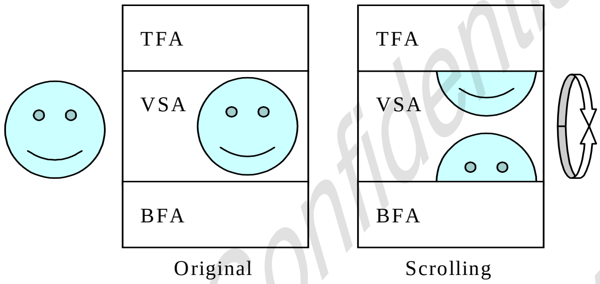
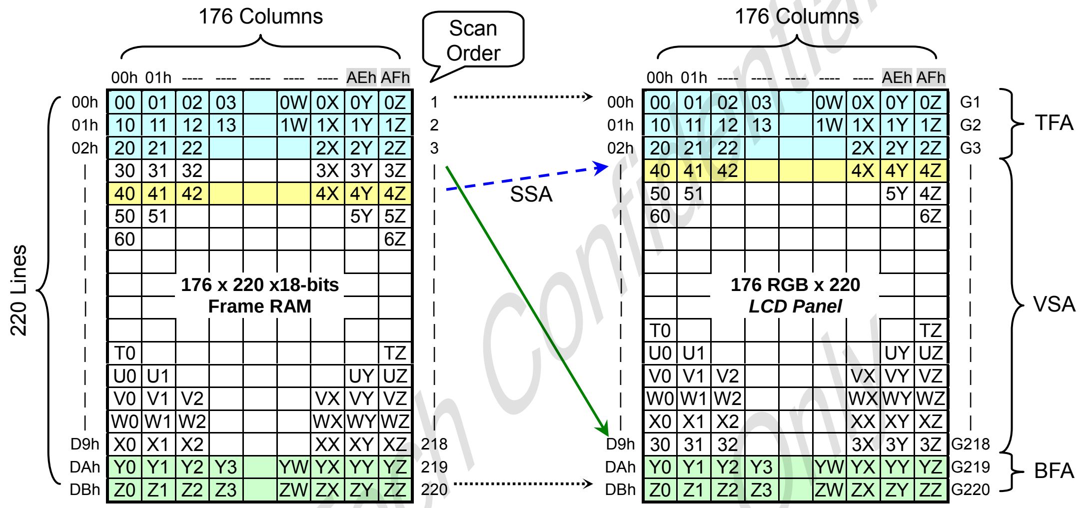


Fig. 7.5.4.1 Difference between Scrolling and original

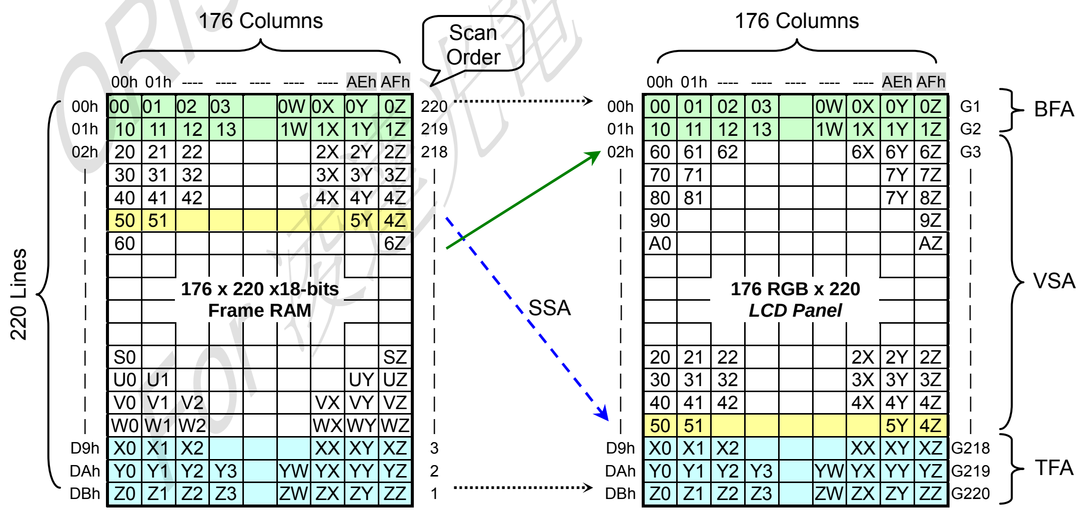
7.5.4.1. When using 176RGB x 220 resolution (GM1, GM0 = “00”)

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=220. In this case, scrolling is applied as shown below.

(1) Example for TFA =3, VSA=215, BFA=2, SSA=4, ML=0: Scrolling



(2) Example for TFA =3, VSA=215, BFA=2, SSA=215, ML=1: Scrolling: TFA and BFT are exchanged



7.5.5. Vertical Scroll Example

Vertical Scroll Example (GM1, GM0 = “00”)

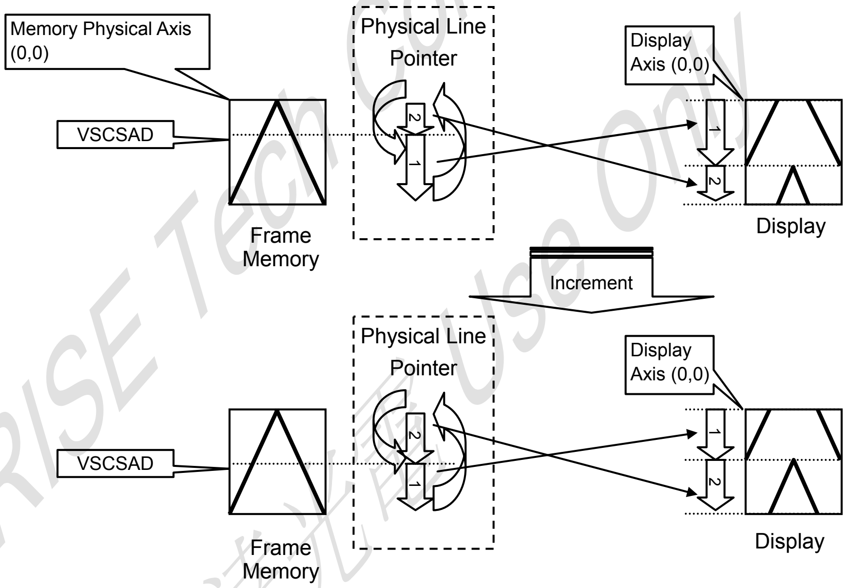
There are 2 types of vertical scrolling, which are determined by the commands “ Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA≠220

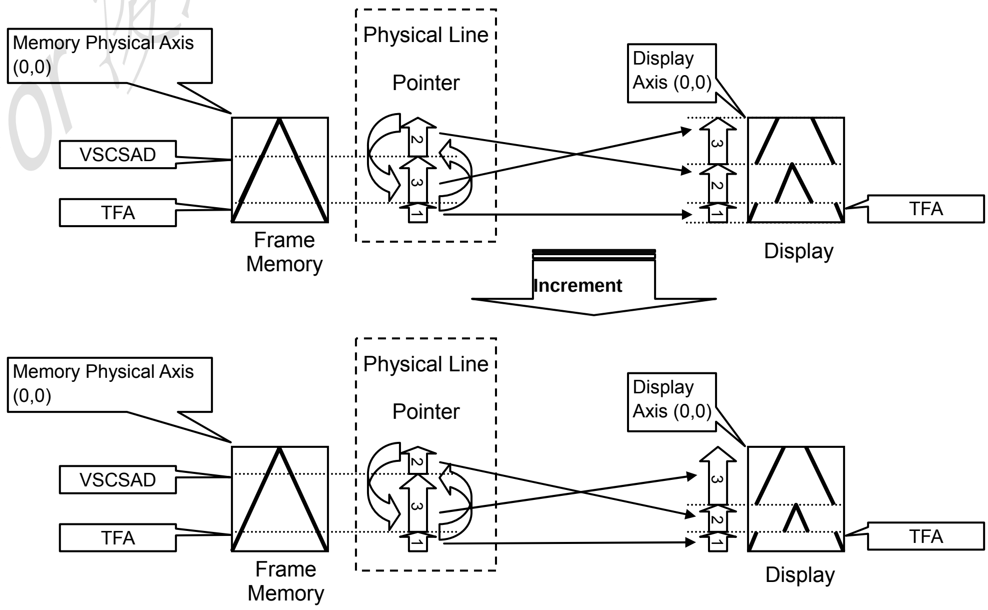
N/A. Do not set TFA + VSA + BFA≠160. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=220 (Scrolling)

Example1) When MADCTR parameter ML=”0”, TFA=0, VSA=220, BFA=0 and VSCSAD=80.



Example2) When MADCTR parameter ML=”1”, TFA=30, VSA=190, BFA=0 and VSCSAD=80.



7.6. Address Counter

The address counter sets the addresses of the display data RAM for writing and reading. (Example for GM1, GM0 = “00”)

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 8-8-8-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=175 (AFh) and Y=0 to Y=219 (DBh). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=175 (AFh), YE=219 (DBh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

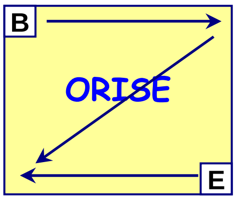
For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR” , define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 6.6.1 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as Fig. 7.6.1 below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

7.7. Memory Data Write/ Read Direction

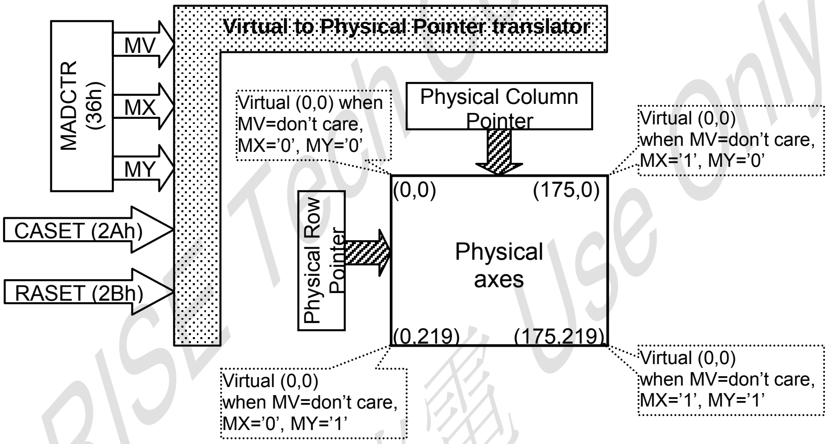
The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.



Data Stream order is like in this figure

Fig. 7.7.1 Data streaming order

-When 176RGBx220 (GM=’00’)

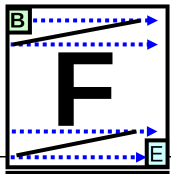
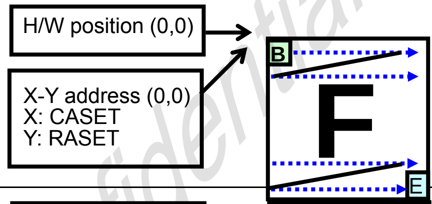
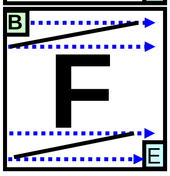
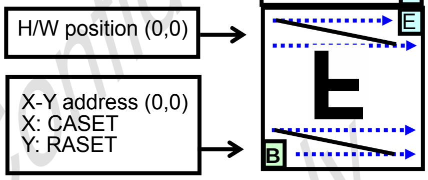
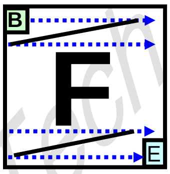
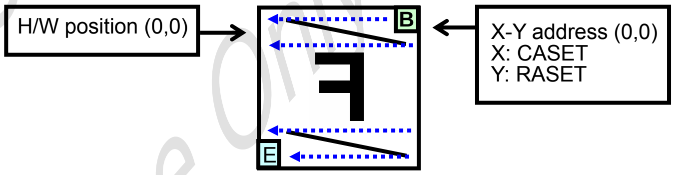
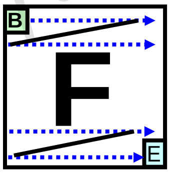
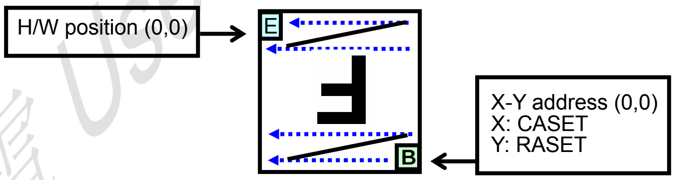
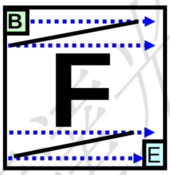
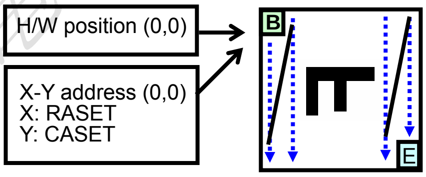
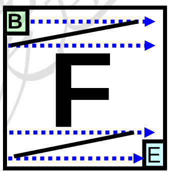
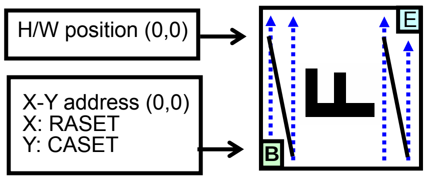
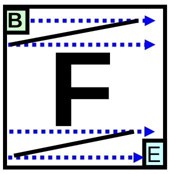
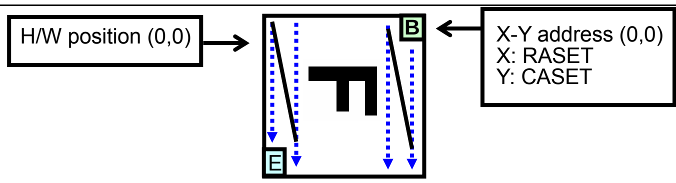
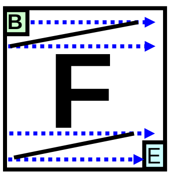
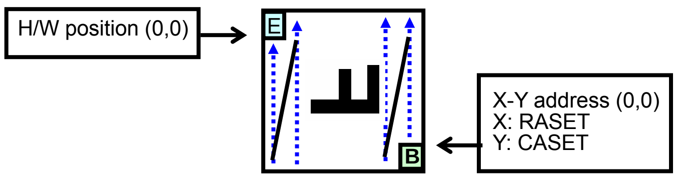


MV	MX	MV	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (219-Physical Row Pointer)
0	1	0	Direct to (127-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (127-Physical Column Pointer)	Direct to (219-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (175-Physical Column Pointer)
1	1	1	Direct to (159-Physical Row Pointer)	Direct to (175-Physical Column Pointer)

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

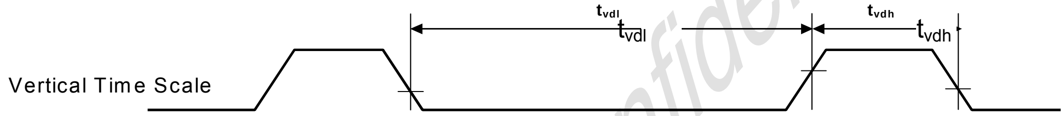
Display Data Direction	MADCTR Parameter MV	MX	MY	Image in the Host (MPU)	Image in the Driver (DDRAM)
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

7.8. Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.8.1. Tearing Effect Line Modes

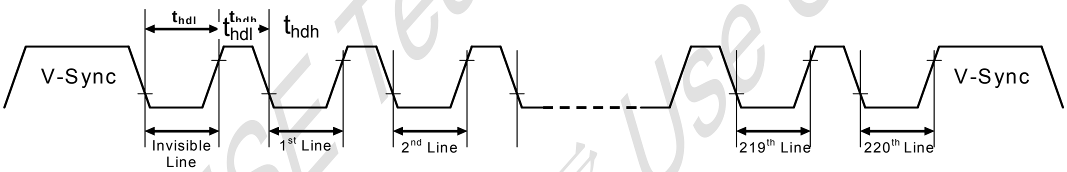
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh}= The LCD display is not updated from the Frame Memory

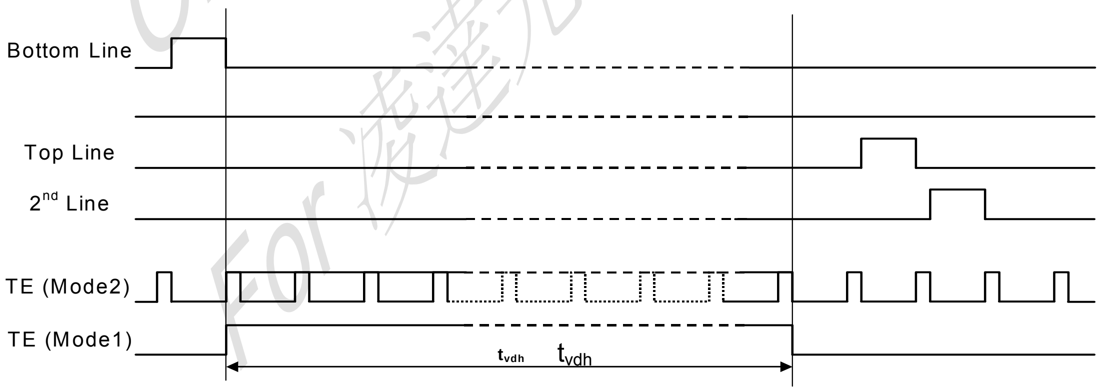
t_{vdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory

t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

7.8.2. Tearing Effect Line Timings

The Tearing Effect signal is described below:

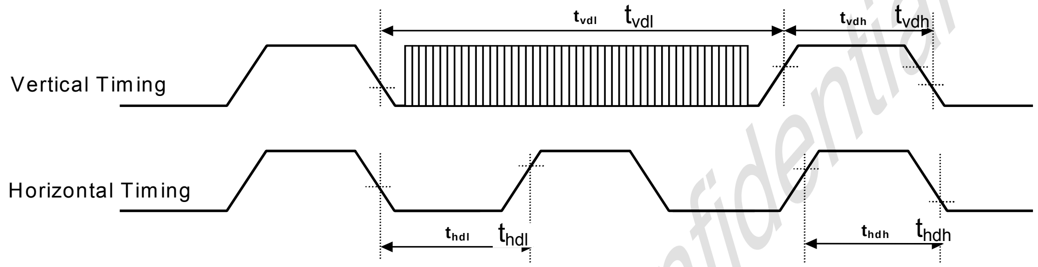


Table 7.8.2.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 58.9 Hz)

Symbol	Parameter	min	max	unit	description
t_{vdl}	Vertical Timing Low Duration	13	-	ms	
t_{vdh}	Vertical Timing High Duration	1000	-	μs	
t_{hdl}	Horizontal Timing Low Duration	33	-	μs	
t_{hdh}	Horizontal Timing High Duration	25	500	μs	

NOTE: The timings in Table 7.8.2.1 apply when MADCTR ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

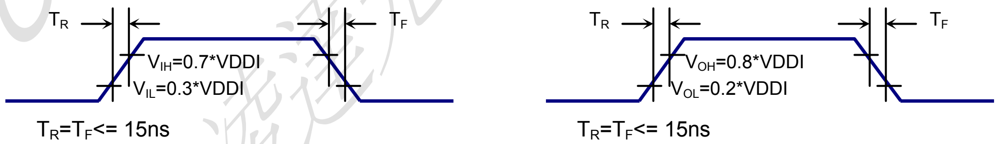
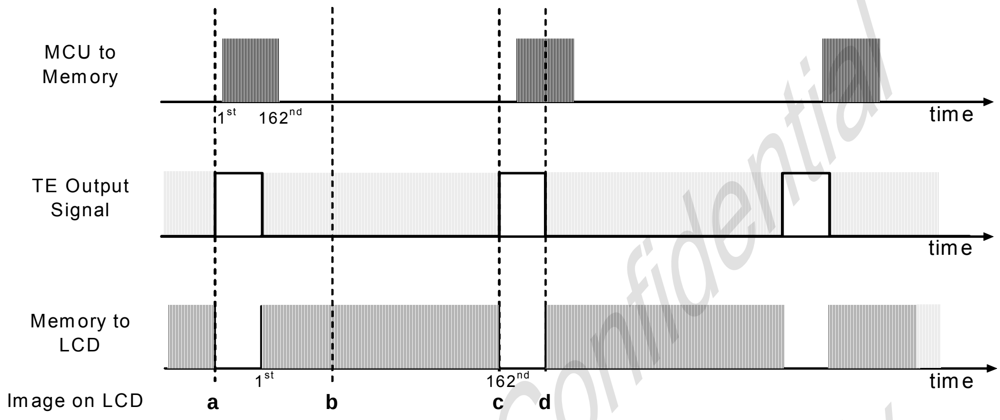


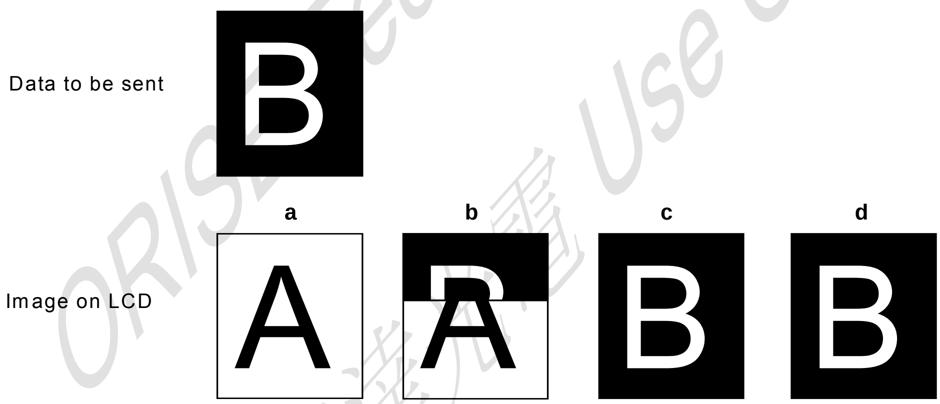
Fig. 7.8.2.2 Rising and Falling timing for Input and Output signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

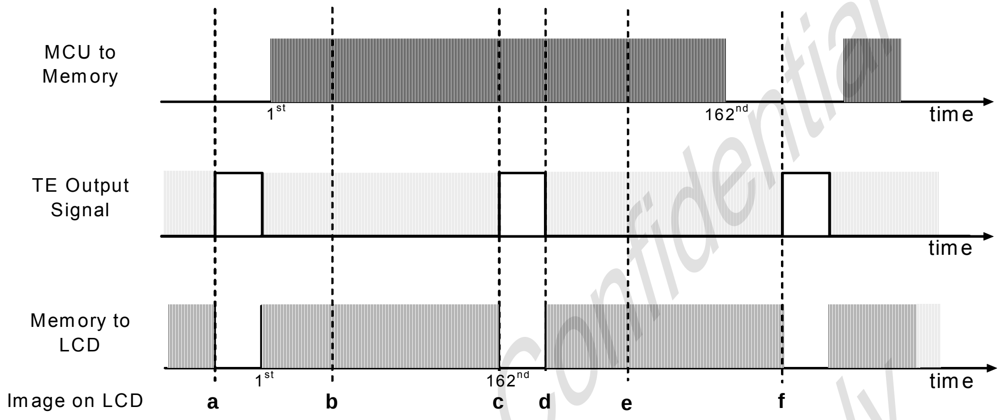
7.8.3. Example 1: MPU Write is faster than panel read.



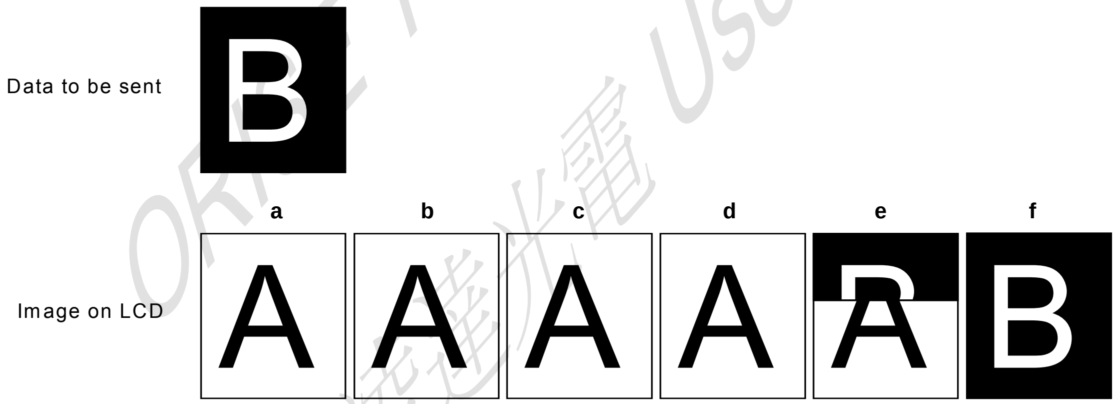
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



7.8.4. Example 2: MPU write is slower than panel read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



7.9. Preset Values

ORISE has already set all preset values in SPFD54126B. Any of these preset values do not need customer's SW support.

7.10. Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDDI and VDD can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

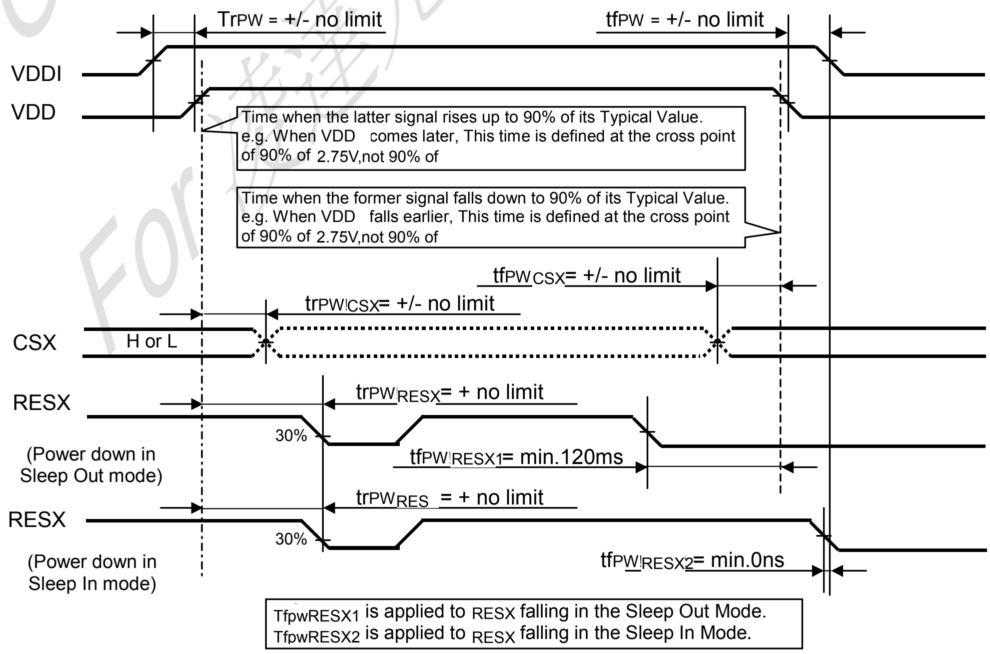
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

7.10.1. Case 1 – RESX Line is held High or Unstable by Host at Power On

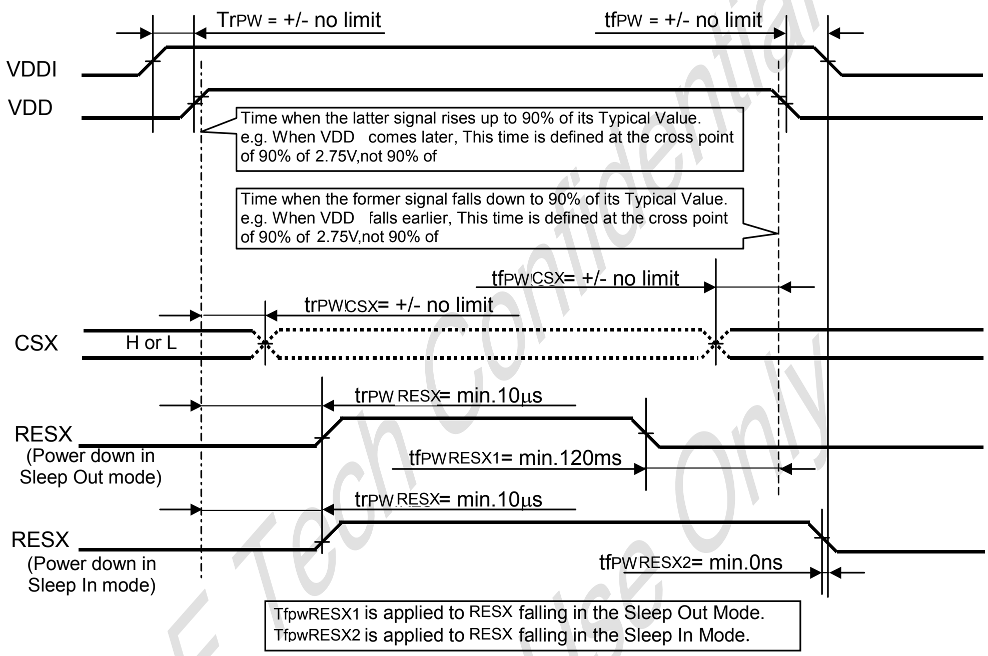
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.10.2. Case 2 – RESX Line is Held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD and VDDI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.10.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

7.11. Power Level Definition

7.11.1. Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode

In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

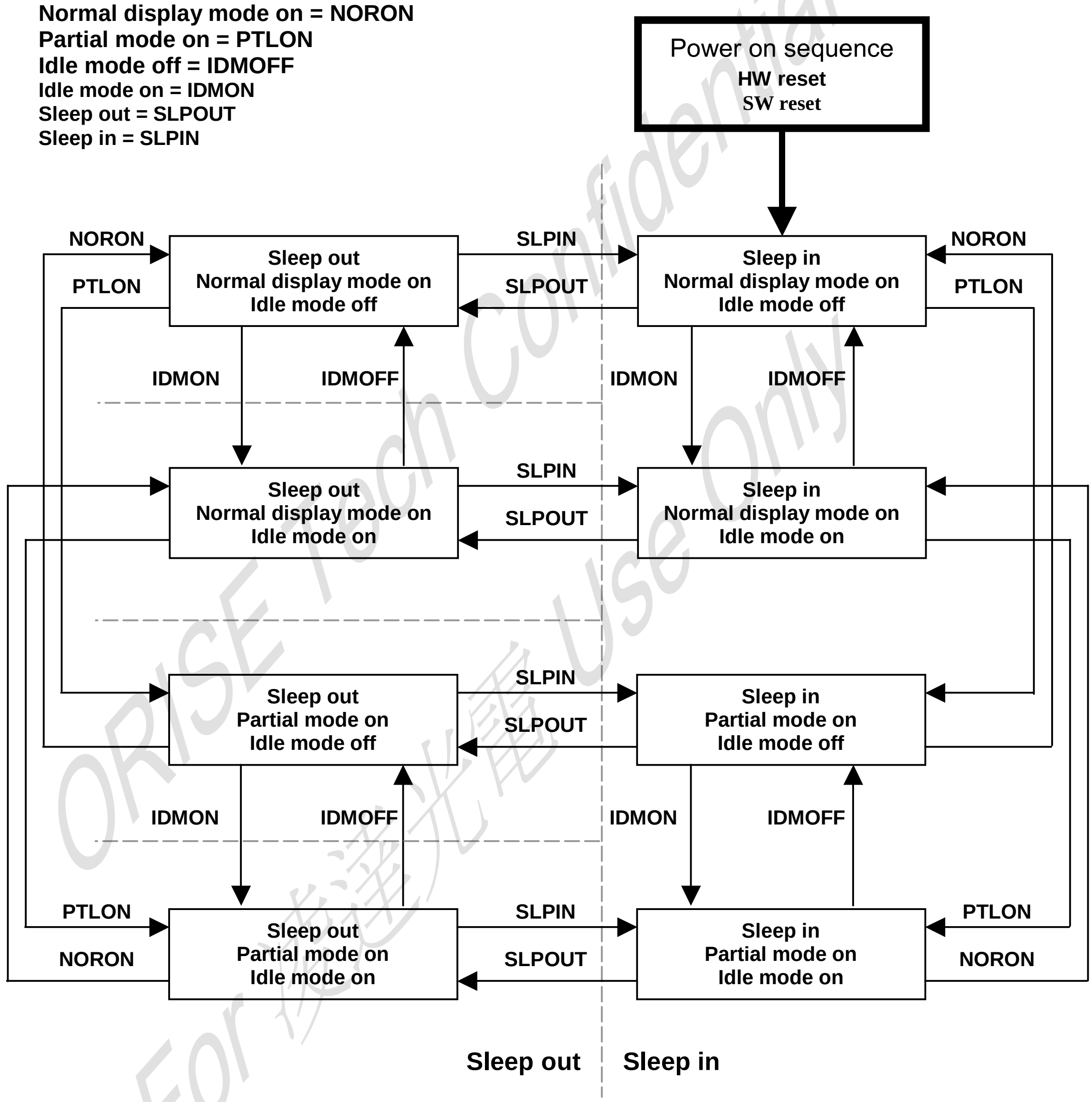
6. Power Off Mode

In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

7.11.2. Power Flow Chart

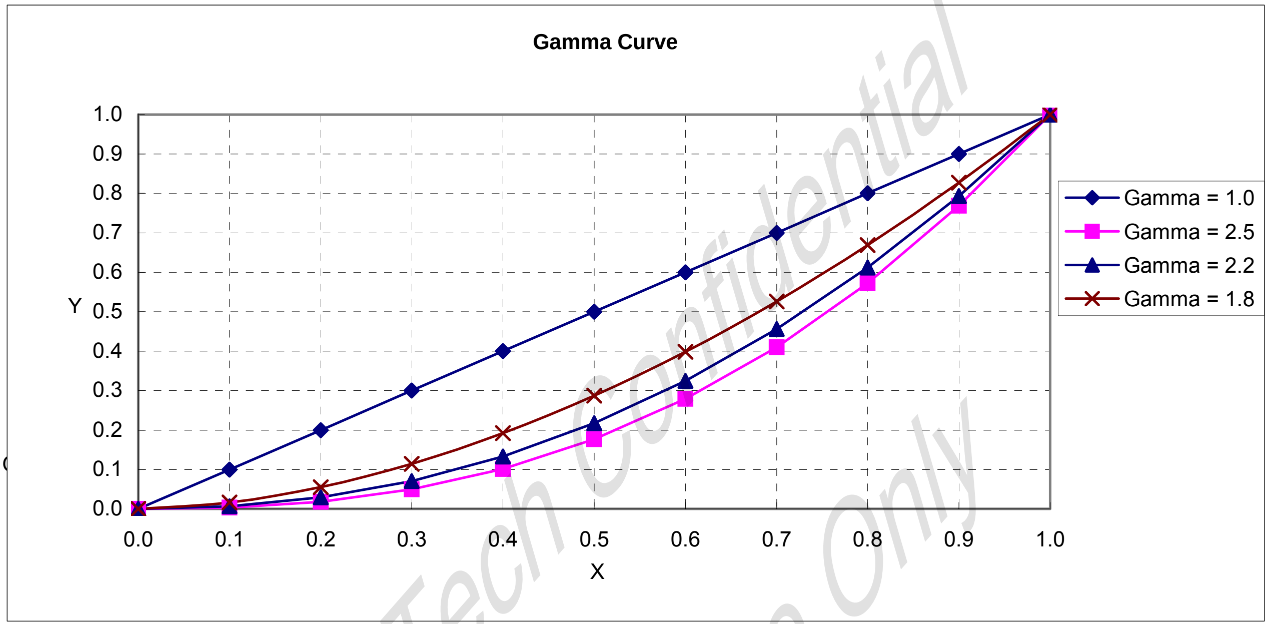
Normal display mode on = NORON
Partial mode on = PTLON
Idle mode off = IDMOFF
Idle mode on = IDMON
Sleep out = SLPOUT
Sleep in = SLPIN



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

7.12. Gamma Curves



7.13. Reset

7.13.1. Reset Value

7.13.1.1. Reset Table (Default Value, GM=00, 176RGB x 220)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	00AFh	00AFh	00AFh (175d) (when MV=0) 00DBh (219d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00DBh	00DBh	00DBh (219d) (when MV=0) 00AFh (175d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 6.14	See Section 6.14	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00DBh	00DBh	00DBh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00DBh	00DBh	00DBh
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	80h	80h	80h
ID3	62h	62h	62h

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDI are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

7.13.1.2. Reset Table (GM=01, 176RGB x 176)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	00AFh	00AFh	00AFh (175d) (when MV=0) 00AFh (175d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00DBh	00DBh	00AFh (175d) (when MV=0) 00AFh (175d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 6.14	See Section 6.14	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00AFh	00AFh	00AFh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00AFh	00AFh	00AFh
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	80h	80h	80h
ID3	62h	62h	62h

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDI are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

7.13.1.3. Reset Table (GM=11, 176RGB x 132)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	00AFh	00AFh	00AFh (175d) (when MV=0) 0083h (131d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00DBh	00DBh	0083h (131d) (when MV=0) 00AFh (175d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 6.14	See Section 6.14	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	0083h	0083h	0083h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	0083h	0083h	0083h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	80h	80h	80h
ID3	62h	62h	62h

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDI are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

7.13.2. Module Input/Output Pins

7.13.2.1. Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D7 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

7.13.2.2. Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 6.10	Input valid	Input valid	Input valid	See 6.10
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D7 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid
P/SX	Input invalid	Input valid	Input valid	Input valid	Input invalid

7.13.3. Reset Timing

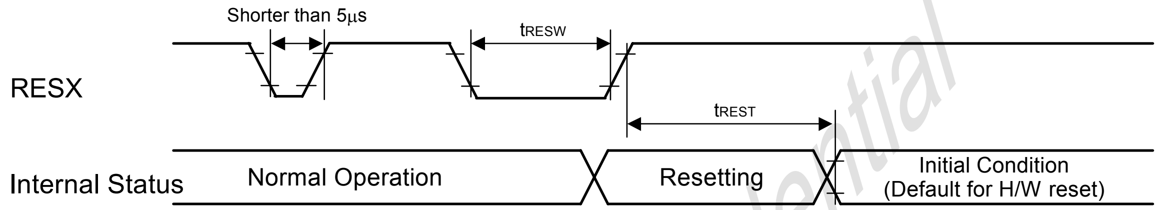


Table 7.13.3.1 Reset input timing

VSS=0V, VDDI=1.6V to 3.6V, VDD=2.6V to 3.5V,Ta = -30 to 70°C)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

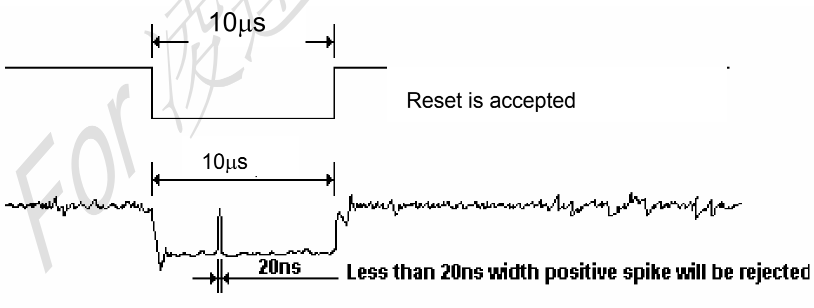
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.14. Colour Depth Conversion Look Up Tables

7.14.1. 4096 and 65536 Colour to 262,144 Colour

Colour	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset		RGBSET Parameter	Look Up Table Input Data	
		4k Colour	65k Colour		4k Colour	65k Colour
RED	$R_{005}R_{004}R_{003}R_{002}R_{001}R_{000}$	000000	000000	1	0000	00000
	$R_{015}R_{014}R_{013}R_{012}R_{011}R_{010}$	000100	000010	2	0001	00001
	$R_{025}R_{024}R_{023}R_{022}R_{021}R_{020}$	001000	000100	3	0010	00010
	$R_{035}R_{034}R_{033}R_{032}R_{031}R_{030}$	001100	000110	4	0011	00011
	$R_{045}R_{044}R_{043}R_{042}R_{041}R_{040}$	010001	001000	5	0100	00100
	$R_{055}R_{054}R_{053}R_{052}R_{051}R_{050}$	010101	001010	6	0101	00101
	$R_{065}R_{064}R_{063}R_{062}R_{061}R_{060}$	011001	001100	7	0110	00110
	$R_{075}R_{074}R_{073}R_{072}R_{071}R_{070}$	011101	001110	8	0111	00111
	$R_{085}R_{084}R_{083}R_{082}R_{081}R_{080}$	100010	010000	9	1000	01000
	$R_{095}R_{094}R_{093}R_{092}R_{091}R_{090}$	100110	010010	10	1001	01001
	$R_{105}R_{104}R_{103}R_{102}R_{101}R_{100}$	101010	010100	11	1010	01010
	$R_{115}R_{114}R_{113}R_{112}R_{111}R_{110}$	101110	010110	12	1011	01011
	$R_{125}R_{124}R_{123}R_{122}R_{121}R_{120}$	110011	011000	13	1100	01100
	$R_{135}R_{134}R_{133}R_{132}R_{131}R_{130}$	110111	011010	14	1101	01101
	$R_{145}R_{144}R_{143}R_{142}R_{141}R_{140}$	111011	011100	15	1110	01110
	$R_{155}R_{154}R_{153}R_{152}R_{151}R_{150}$	111111	011110	16	1111	01111
	$R_{165}R_{164}R_{163}R_{162}R_{161}R_{160}$	Not Used	100001	17	Not Used	10000
	$R_{175}R_{174}R_{173}R_{172}R_{171}R_{170}$		100011	18		10001
	$R_{185}R_{184}R_{183}R_{182}R_{181}R_{180}$		100101	19		10010
	$R_{195}R_{194}R_{193}R_{192}R_{191}R_{190}$		100111	20		10011
	$R_{205}R_{204}R_{203}R_{202}R_{201}R_{200}$		101001	21		10100
	$R_{215}R_{214}R_{213}R_{212}R_{211}R_{210}$		101011	22		10101
	$R_{225}R_{224}R_{223}R_{222}R_{221}R_{220}$		101101	23		10110
	$R_{235}R_{234}R_{233}R_{232}R_{231}R_{230}$		101111	24		10111
	$R_{245}R_{244}R_{243}R_{242}R_{241}R_{240}$		110001	25		11000
	$R_{255}R_{254}R_{253}R_{252}R_{251}R_{250}$		110011	26		11001
	$R_{265}R_{264}R_{263}R_{262}R_{261}R_{260}$		110101	27		11010
	$R_{275}R_{274}R_{273}R_{272}R_{271}R_{270}$		110111	28		11011
	$R_{285}R_{284}R_{283}R_{282}R_{281}R_{280}$		111001	29		11100
	$R_{295}R_{294}R_{293}R_{292}R_{291}R_{290}$		111011	30		11101
	$R_{305}R_{304}R_{303}R_{302}R_{301}R_{300}$		111101	31		11110
	$R_{315}R_{314}R_{313}R_{312}R_{311}R_{310}$		111111	32		11111

Colour	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset		RGBSET Parameter	Look Up Table Input Data	
		4k Colour	65k Colour		4k Colour	65k Colour
GREEN	$G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}$	000000	000000	33	0000	000000
	$G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}$	000100	000001	34	0001	000001
	$G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}$	001000	000010	35	0010	000010
	$G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}$	001100	000011	36	0011	000011
	$G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}$	010001	000100	37	0100	000100
	$G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}$	010101	000101	38	0101	000101
	$G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}$	011001	000110	39	0110	000110
	$G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}$	011101	000111	40	0111	000111
	$G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}$	100010	001000	41	1000	001000
	$G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}$	100110	001001	42	1001	001001
	$G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}$	101010	001010	43	1010	001010
	$G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}$	101110	001011	44	1011	001011
	$G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}$	110011	001100	45	1100	001100
	$G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}$	110111	001101	46	1101	001101
	$G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}$	111011	001110	47	1110	001110
	$G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}$	111111	001111	48	1111	001111
	$G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}$	Not Used	010000	49	Not Used	010000
	$G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}$		010001	50		010001
	$G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}$		010010	51		010010
	$G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}$		010011	52		010011
	$G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}$		010100	53		010100
	$G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}$		010101	54		010101
	$G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}$		010110	55		010110
	$G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}$		010111	56		010111
	$G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}$		011000	57		011000
	$G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}$		011001	58		011001
	$G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}$		011010	59		011010
	$G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}$		011011	60		011011
	$G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}$		011100	61		011100
	$G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}$		011101	62		011101
	$G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}$		011110	63		011110
	$G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}$		011111	64		011111

Colour	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset		RGBSET parameter	Look Up Table Input Data	
		4k Colour	65k Colour		4k Colour	65k Colour
GREEN	$G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}$	Not Used	100000	65	Not Used	100000
	$G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}$		100001	66		100001
	$G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}$		100010	67		100010
	$G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}$		100011	68		100011
	$G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}$		100100	69		100100
	$G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}$		100101	70		100101
	$G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}$		100110	71		100110
	$G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}$		100111	72		100111
	$G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}$		101000	73		101000
	$G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}$		101001	74		101001
	$G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}$		101010	75		101010
	$G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}$		101011	76		101011
	$G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}$		101100	77		101100
	$G_{455} G_{454} G_{453} G_{452} G_{451} G_{450}$		101101	78		101101
	$G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}$		101110	79		101110
	$G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}$		101111	80		101111
	$G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}$		110000	81		110000
	$G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}$		110001	82		110001
	$G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}$		110010	83		110010
	$G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}$		110011	84		110011
	$G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}$		110100	85		110100
	$G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}$		110101	86		110101
	$G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}$		110110	87		110110
	$G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}$		110111	88		110111
	$G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}$		111000	89		111000
	$G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}$		111001	90		111001
	$G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}$		111010	91		111010
	$G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}$		111011	92		111011
	$G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}$		111100	93		111100
	$G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}$		111101	94		111101
	$G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}$		111110	95		111110
	$G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}$		111111	96		111111

Colour	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset 4k Colour	Default value after H/W Reset 65k Colour	RGBSET parameter	Look Up Table Input Data 4k Colour	Look Up Table Input Data 65k Colour
BLUE	$B_{005}B_{004}B_{003}B_{002}B_{001}B_{000}$	000000	000000	97	0000	00000
	$B_{015}B_{014}B_{013}B_{012}B_{011}B_{010}$	000100	000011	98	0001	00001
	$B_{025}B_{024}B_{023}B_{022}B_{021}B_{020}$	001000	000101	99	0010	00010
	$B_{035}B_{034}B_{033}B_{032}B_{031}B_{030}$	001100	000111	100	0011	00011
	$B_{045}B_{044}B_{043}B_{042}B_{041}B_{040}$	010001	001001	101	0100	00100
	$B_{055}B_{054}B_{053}B_{052}B_{051}B_{050}$	010101	001011	102	0101	00101
	$B_{065}B_{064}B_{063}B_{062}B_{061}B_{060}$	011001	001101	103	0110	00110
	$B_{075}B_{074}B_{073}B_{072}B_{071}B_{070}$	011101	001111	104	0111	00111
	$B_{085}B_{084}B_{083}B_{082}B_{081}B_{080}$	100010	010001	105	1000	01000
	$B_{095}B_{094}B_{093}B_{092}B_{091}B_{090}$	100110	010011	106	1001	01001
	$B_{105}B_{104}B_{103}B_{102}B_{101}B_{100}$	101010	010101	107	1010	01010
	$B_{115}B_{114}B_{113}B_{112}B_{111}B_{110}$	101110	010111	108	1011	01011
	$B_{125}B_{124}B_{123}B_{122}B_{121}B_{120}$	110011	011001	109	1100	01100
	$B_{135}B_{134}B_{133}B_{132}B_{131}B_{130}$	110111	011011	110	1101	01101
	$B_{145}B_{144}B_{143}B_{142}B_{141}B_{140}$	111011	011101	111	1110	01110
	$B_{155}B_{154}B_{153}B_{152}B_{151}B_{150}$	111111	011111	112	1111	01111
	$B_{165}B_{164}B_{163}B_{162}B_{161}B_{160}$	Not Used	100001	113	Not Used	10000
	$B_{175}B_{174}B_{173}B_{172}B_{171}B_{170}$		100011	114		10001
	$B_{185}B_{184}B_{183}B_{182}B_{181}B_{180}$		100101	115		10010
	$B_{195}B_{194}B_{193}B_{192}B_{191}B_{190}$		100111	116		10011
	$B_{205}B_{204}B_{203}B_{202}B_{201}B_{200}$		101001	117		10100
	$B_{215}B_{214}B_{213}B_{212}B_{211}B_{210}$		101011	118		10101
	$B_{225}B_{224}B_{223}B_{222}B_{221}B_{220}$		101101	119		10110
	$B_{235}B_{234}B_{233}B_{232}B_{231}B_{230}$		101111	120		10111
	$B_{245}B_{244}B_{243}B_{242}B_{241}B_{240}$		110001	121		11000
	$B_{255}B_{254}B_{253}B_{252}B_{251}B_{250}$		110011	122		11001
	$B_{265}B_{264}B_{263}B_{262}B_{261}B_{260}$		110101	123		11010
	$B_{275}B_{274}B_{273}B_{272}B_{271}B_{270}$		110111	124		11011
	$B_{285}B_{284}B_{283}B_{282}B_{281}B_{280}$		111001	125		11100
	$B_{295}B_{294}B_{293}B_{292}B_{291}B_{290}$		111011	126		11101
	$B_{305}B_{304}B_{303}B_{302}B_{301}B_{300}$		111101	127		11110
	$B_{315}B_{314}B_{313}B_{312}B_{311}B_{310}$		111111	128		11111

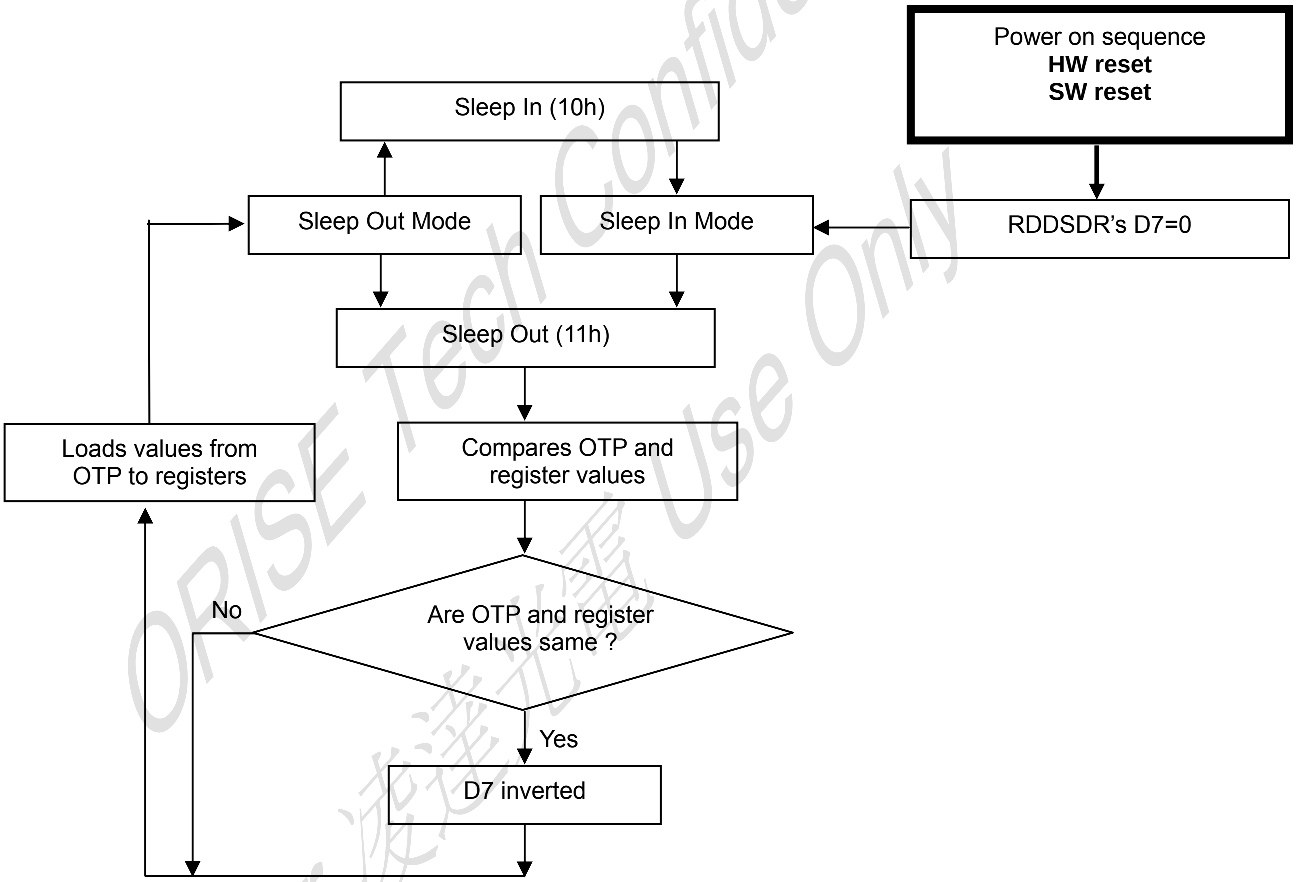
7.15. Sleep Out-Command and Self-Diagnostic Functions of the Display Module

7.15.1. Register Loading Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (one-time programming memory) to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit in "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



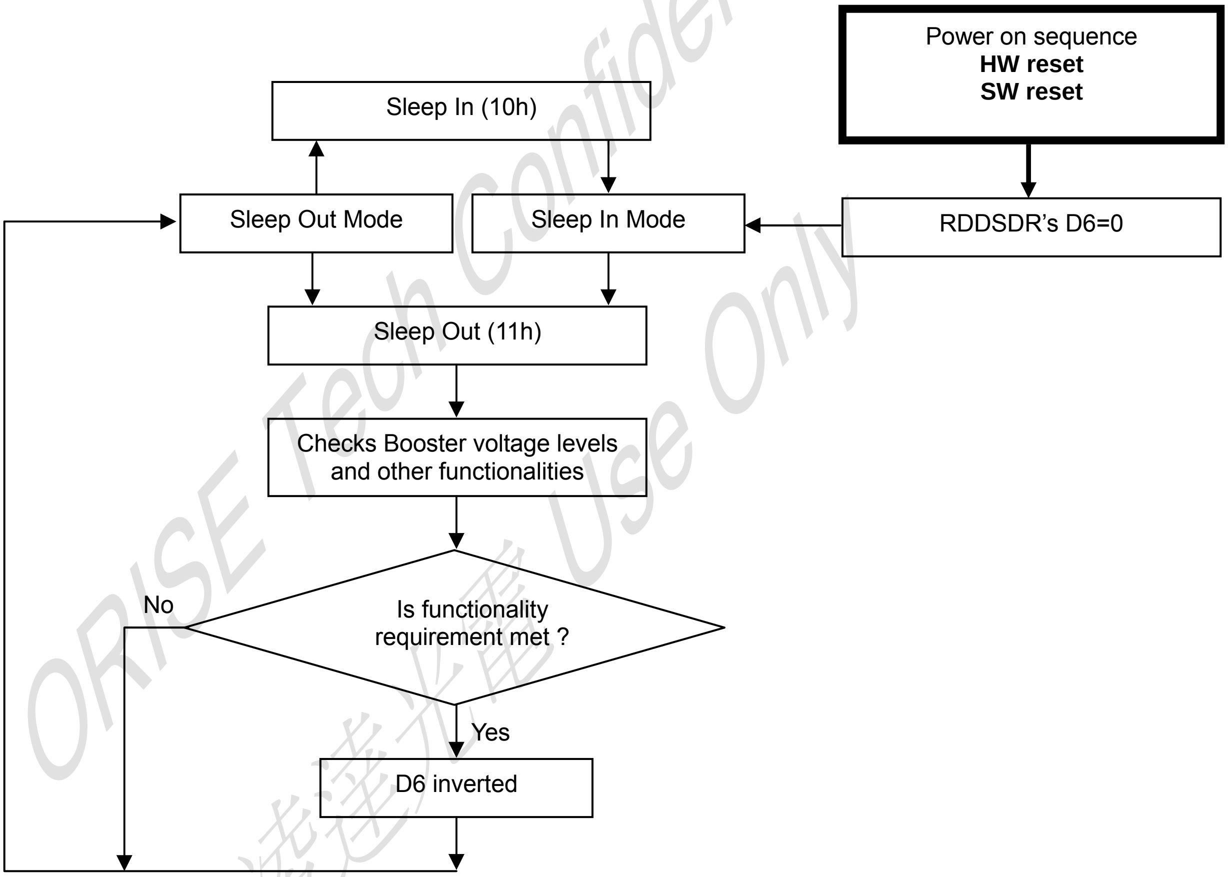
Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

7.15.2. Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit in "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



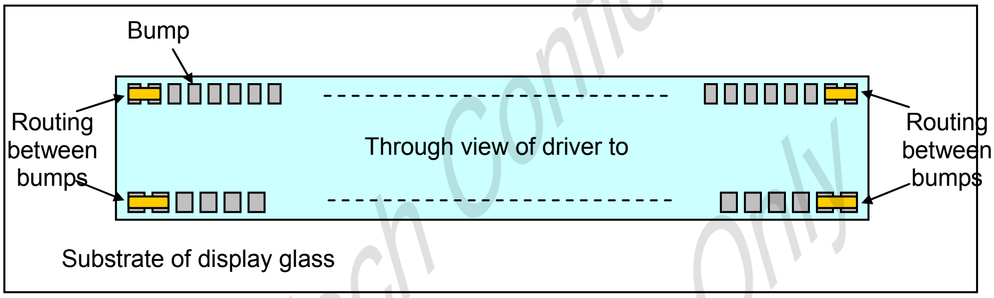
Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

7.15.3. Chip Attachment Detection

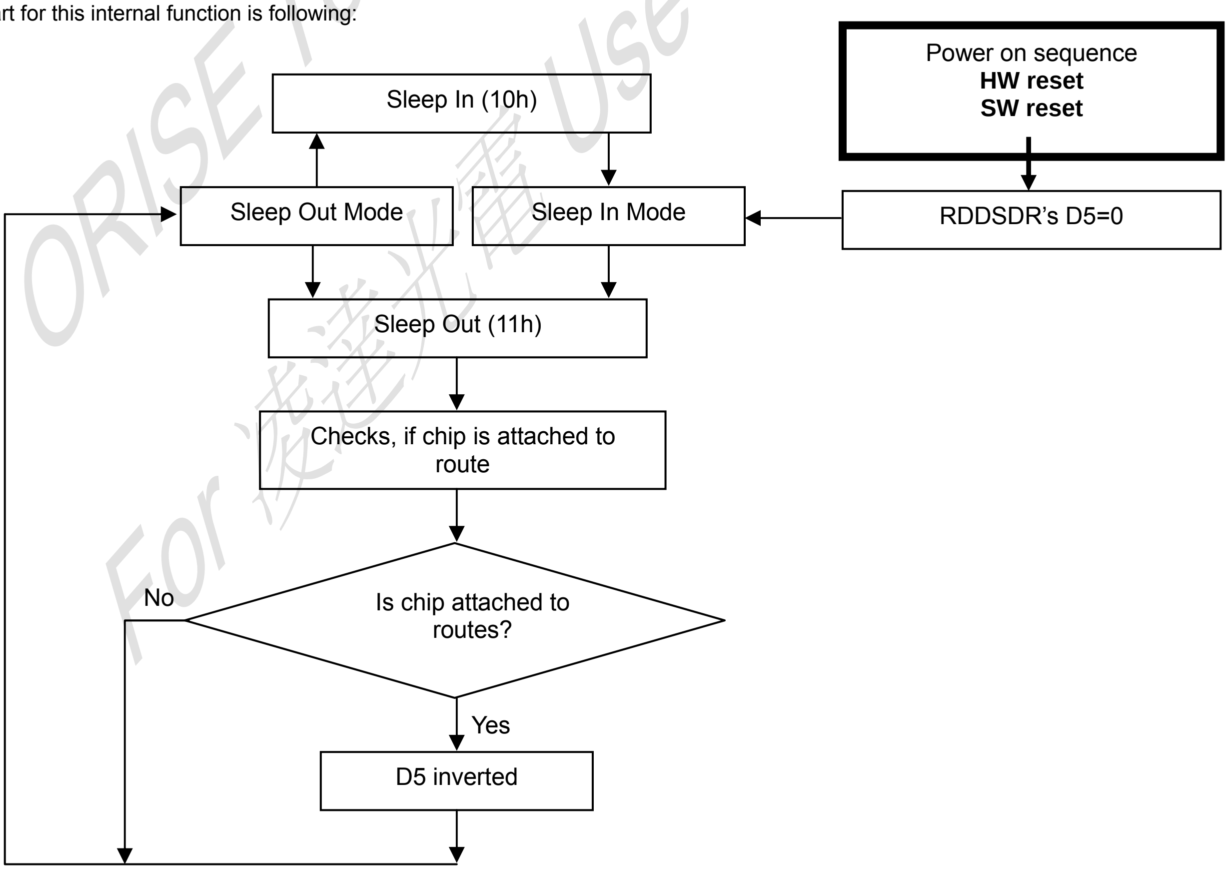
Sleep Out-command is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= increased by 1).

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



The flow chart for this internal function is following:

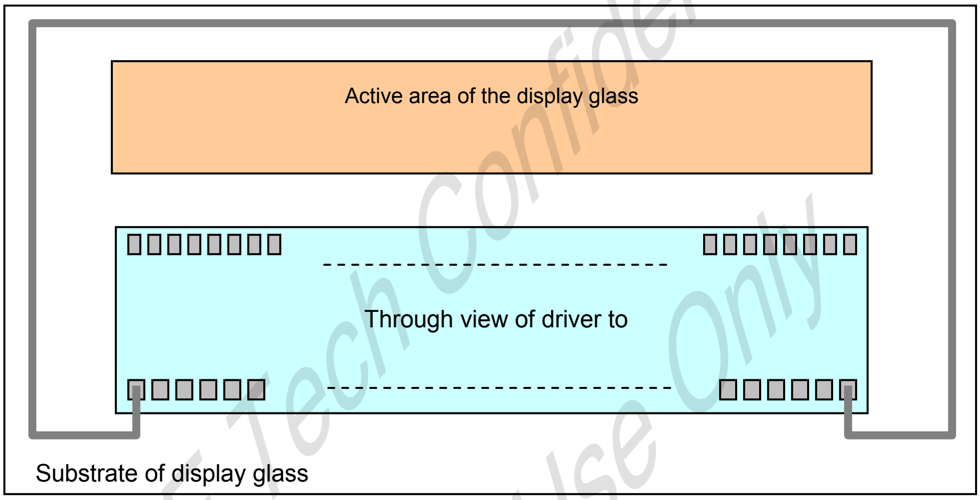


7.15.4. Display Glass Break Detection

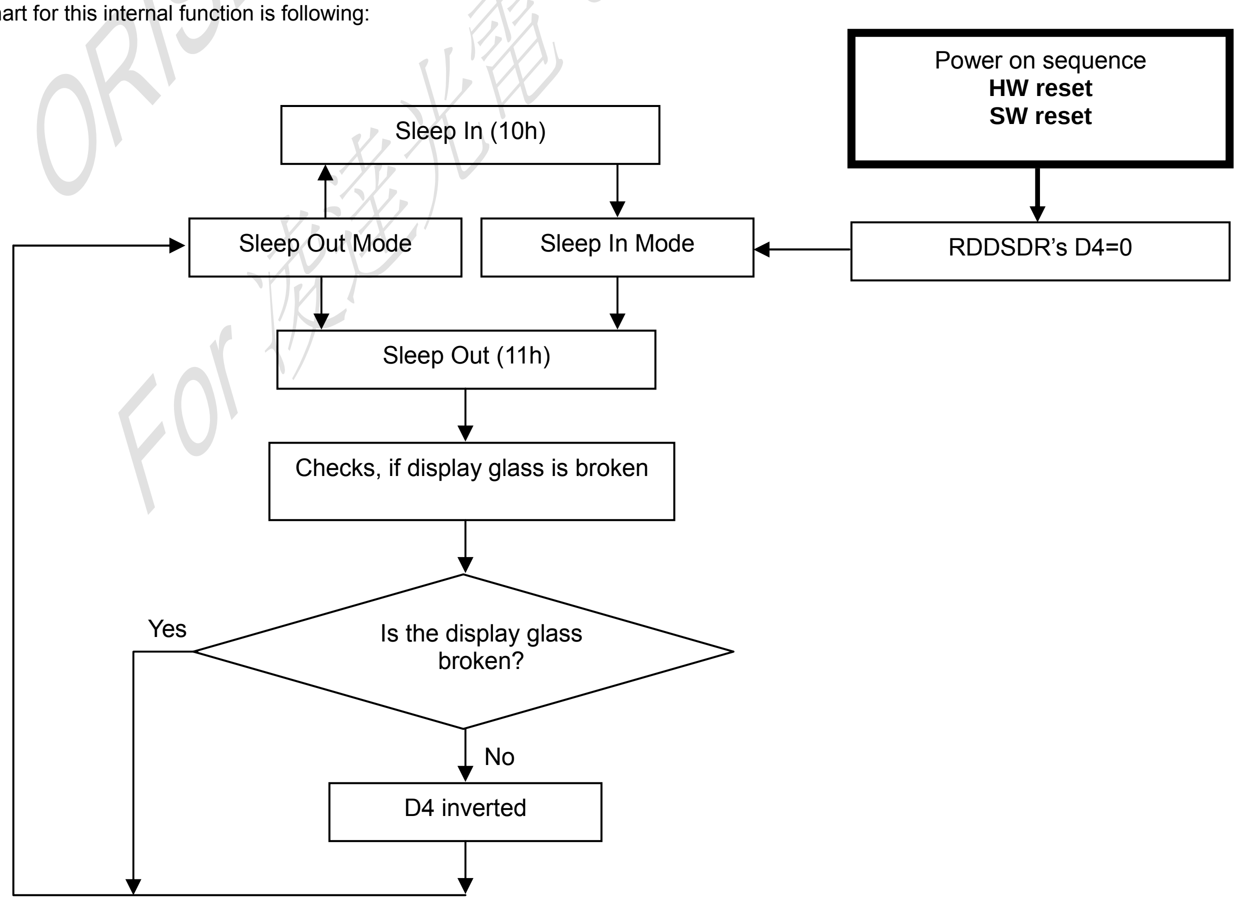
Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

There is inverted (= increased by 1) a bit in "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D4), if the display glass is not broken. If this display glass is broken, this bit (D4) is not inverted (= increased by 1).

The following figure is a reference, how this glass break detection can be implemented e.g. there is connected together 2 bumps via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



The flow chart for this internal function is following:



7.16. Oscillator

The chip has on-chip oscillator that does not require external components. This oscillator output signal is used for system clock generation for internal display operation.

7.17. System Colck Generator

The timing generator produces the various signals to dirver the internal circuitty. Internal chip operation is not affected by operations on the data bus.

7.18. Instruction Decoder and Register

The instruction decoder indentifies command words arriving at the interface and routes the following data bytes to their destination. The command set can be found in " Command" section.

7.19. Source Driver

The source driver block includes 176x3 source outputs (S1 to S528), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simulatance selected rows.

7.20. Gate Driver

The gate dirver block include 220 chanel gate output (G1 to G220) which should be connected directly to the TFT-LCD.

7.20.1. Gate Driver

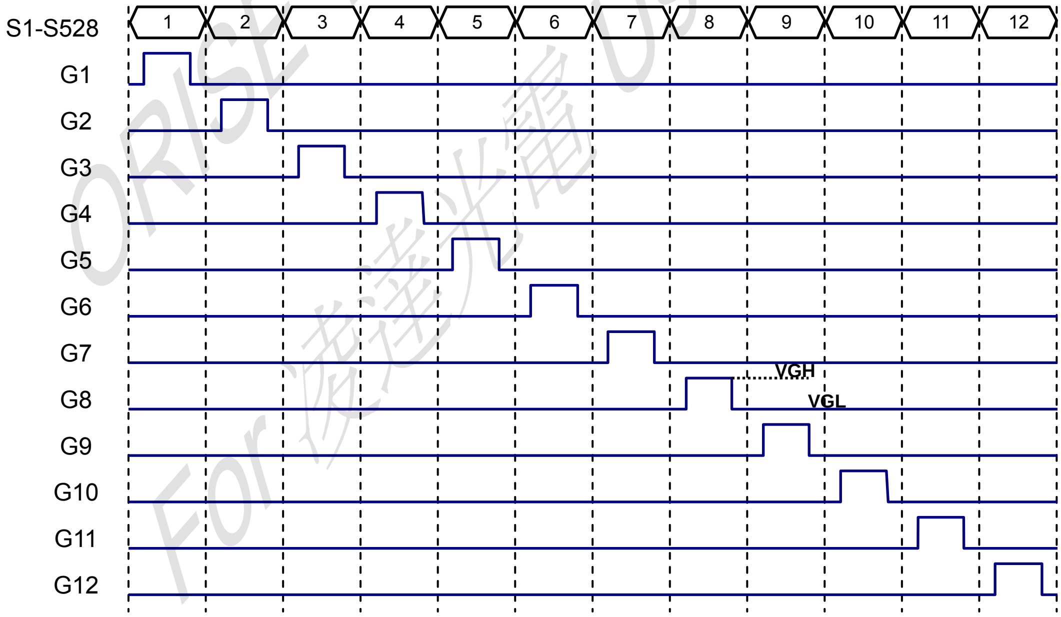


Fig. 7.20.1 Gate Driver Output Option 1

7.21. γ-CORRECTION FUNCTION

The SPFD54126B adopts true 6-bit OP-AMP with adjustable γ-correction function to display in 262,144 colors. The adjustable γ-correction can be set by 10 groups of registers to determine eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register group can be set independently to other register groups.

7.22. VSYNC Interface

The SPFD54126 incorporates a VSYNC-I/F, which enables to display a moving picture with only a system interface and frame-synchronizing signal (VS). This interface enables to display moving pictures with minimum modification to a conventional system.

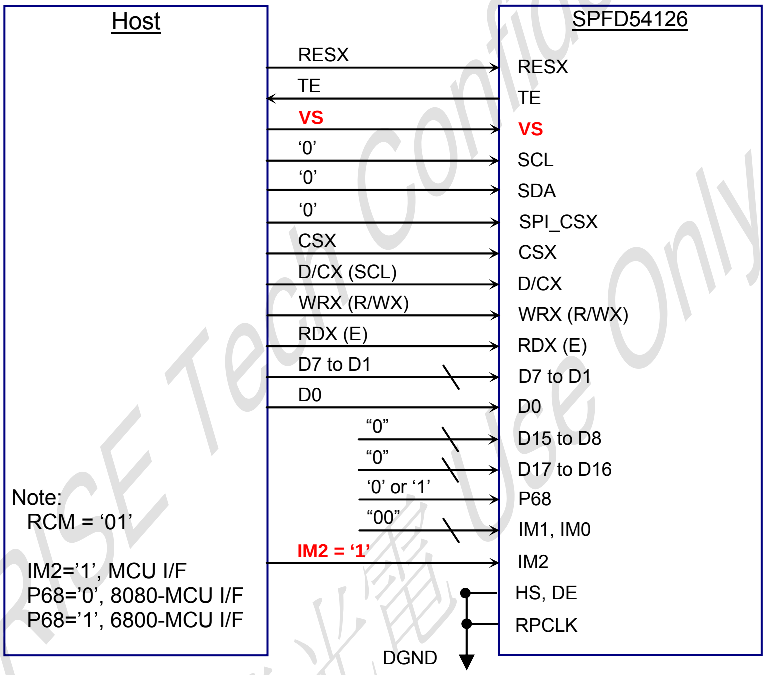
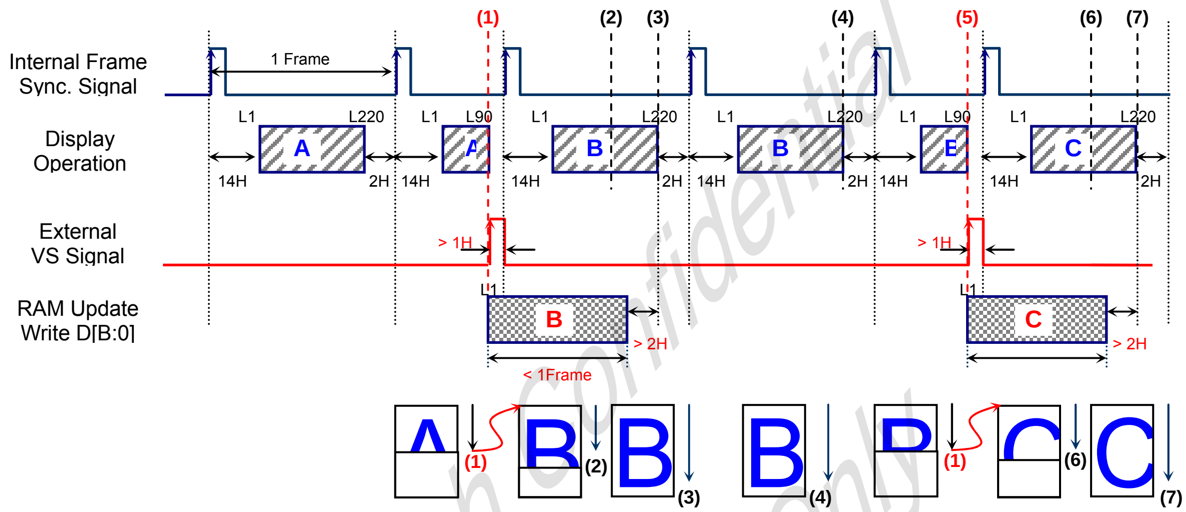


Fig. 7.21.1 VSYNC Interface for 8-bits data bus (Example)

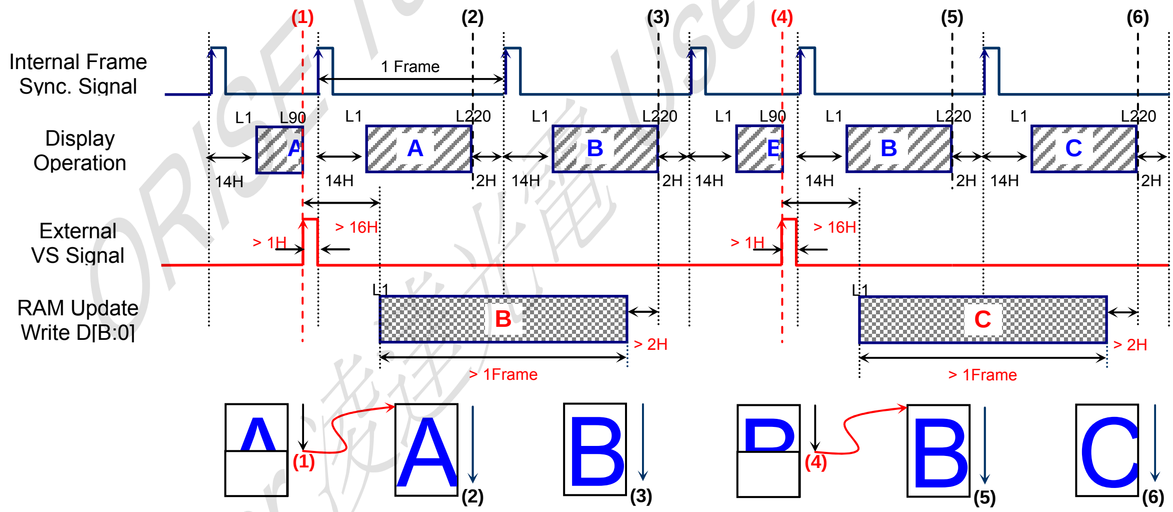
The VSYNC-I/F is truned ON by ***VSYNC-I/F ON (ADH)*** command and turned OFF by ***VSYNC-I/F OFF (ACH)*** command. In VSYNC-I/F mode, internal display operations are synchronized with VS. The VSYNC-I/F enables to display a moving picture through a system interface and update screens without flicker by writing data to RAM through a system interface in higher speed than the internal display operations by some degree.

The VSYNC-I/F executes display operations only with internal clocks generated by internal oscillators and VS input. All display data are stored in RAM so that only the data relevant to updating a screen are transferred to minimize data transmission while displaying a moving picture.

- Leading Mode



- Lagging Mode



1. In RCM1, RCM0 = “01” mode, writing data to RAM on rising edge of VS signal
2. If high pulse of VS signal shoule large than 1-lines.
3. The BP and FP should follow conditions : BP ≧2-lines , FP≧2-lines and BP+FP = 16-lines
4. The signals (CSX, WRX, D/CX and VS) of VSYNC I/F should follow MCU Parallel Interface AC timing.
5. B=17.

The VSYNC-I/F has limits on the minimum RAM write speed through the system interface and the frequency of the internal clocks. It requires a RAM write speed more than the calculated result from the following formula.

- Internal clock frequency (fosc) [Hz]

= Frame Frequency x (DisplayLines +Front Porch(VSFP)+BackPorch (VSBP)) x 16(clocks) x fluctuation

$$\text{RAM Write Speed (Min) (Hz)} = \frac{176 \times Display\ Line(220 Line)}{BackPorch\,(VSBP) + Display\ Line - m\arg ins)x16\,(clocks) \times {}^{1}\!/\!{}_{fosc}}$$

Note 1: When RAM write does not start right after the falling edge of VS, the time from the falling edge of VS until RAM write starts must also be taken into account.

Example of RAMs writes speed and the frequency of the internal clocks in VSYNC-I/F mode is as follows.

Example:

Display size: 176 RGB × 220 lines

Raster-rows: 220 lines

Back/ Front porch: 14/ 2 lines (VSBP = 1110/ VSFP = 0010 of AFH)

-When Frame frequency: 60 Hz

Internal clock frequency (fosc) [Hz] =

60Hz × (220+2+14) lines × 16 Clocks × 1.1 / 0.9 = 277kHz

When calculating an internal clock frequency, possible causes of fluctuations must also be taken into consideration. In this example, the allowance for the fluctuation is ± 10 % from the center value, and the frequency must be within a VS cycle.

Also in this example, variations attributed to LSI fabrication and room temperature are taken into consideration as causes of fluctuations. Other possible causes of fluctuations, such as variations in external resistors or voltage changes are not considered in this example. It is necessary to make a setting with enough margins to accommodate

-When Frame frequency: 60Hz

Minimum speed for RAM writing [Hz] >

176 × 220 / {((14+220-2) lines × 16 clock) / 300 kHz} = 2.89MHz

Note 2: The above calculation is premised on the case of writing data to RAM on the falling edge of VS.

Note 3: There must at least be a margin of 2 processing lines when all one-frame data are written to RAM before the SPFD54126 starts processing display lines.

By writing data to RAM on rising edge of VS signal at speed of 2.89MHz (Frame rate=60Hz) or more, it is possible to overwrite an entire screen without flicker by completing data write operation of a line before it starts display operation of that line.

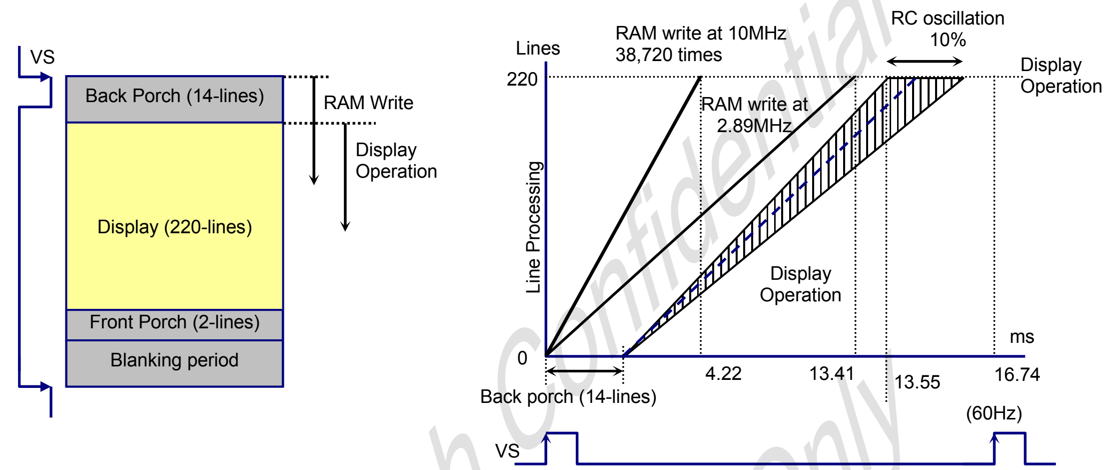


Fig. 7.28.3 Write/Display Operation Timing via VSYNC-I/F

Notes to the VSYNC Interface

1. The aforementioned example of calculation is just a result of calculation. In actual settings, possible causes of fluctuations should be taken into consideration. It is necessary to give enough margins when setting a RAM writing speed.
2. The aforementioned example of calculation is the value in case of overwriting full screen. If a moving picture display area is limited, it will result in more margins between RAMs write and display operations.

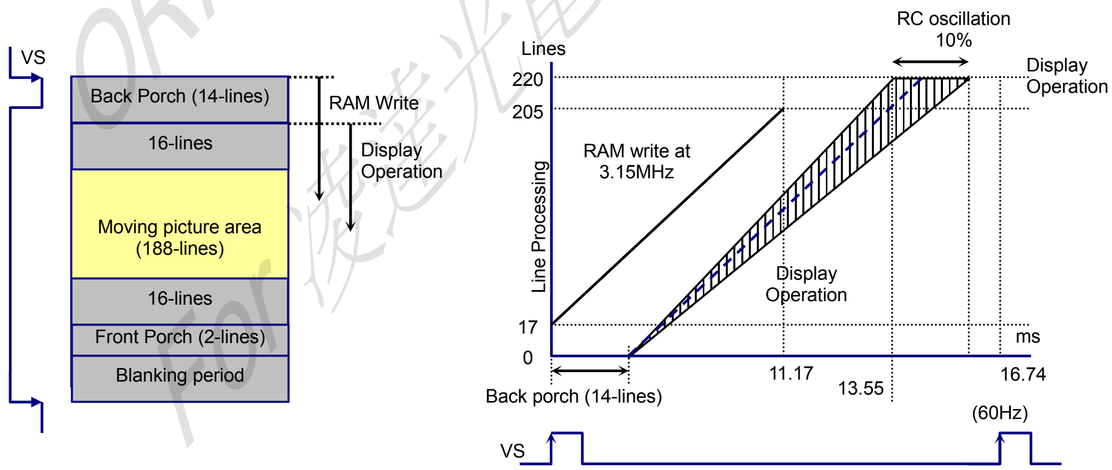


Fig. 7.28.4 RAM write speed margin

3. A front porch period continues after completion of 1 frame and until the next input of VS.
4. The partial display and vertical scroll functions are not available with the VSYNC-I/F.

8. ELECTRICAL SPECIFICATIONS

8.1. DC CharacteristicAC Characteristic (VDD=2.6V~3.0V, VDDIO = 1.6V~3.0V, Ta = -40℃ ~ 85℃)

Parameter	Symbol	Conditions	Specification MIN	TYP	MAX	Unit	Related Pins
Power & Operation Voltage							
Analog Operating voltage	VDD	Operating Voltage	2.6	2.78	3.5	V	Note 2
Logic Operating voltage	VDDI	I/O supply voltage-	1.6	1.8/2.78	3.6	V	Note 2
Gate Driver High voltage	VGH		10.0		13.5	V	Note 3
Gate Driver Low voltage	VGL		-11.5		-9.0	V	Note 3
Driver Supply voltage		|VGH-VGL|	19		30	V	Note 3
Input / Output							
Logic High level input voltage	VIH		0.7VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDI	V	Note 1, 2, 3
Logic High level output voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2VDDI	V	Note 1, 2, 3
Logic High level input current	IIH				1	μA	Note 1, 2, 3
Logic Low level input current	IIL		-1			μA	Note 1, 2, 3
Logic Input leakage current	IIL	VIN = VDDI or VSS	-0.1	-	+0.1	μA	Note 1, 2, 3
VCOM Operation							
VCOM High voltage	VCOMH	Ccom=19nF	2.5		5.0	V	Note 3
VCOM Low voltage	VCOML	Ccom=19nF	-2.5		0.0	V	Note 3
VCOM Amplitude voltage	VCOMA	|VCOMH-VCOML|	4.0		6.0	V	Note 3
Source Driver							
Source output range	VSout		0.1		AVDD-0.1	V	Note 4
Gamma reference voltage	GVDD		3.0		5.0	V	Note 3
Source output settling time	Tr	Below with 99% precision		25	30	μs	Note 4, 5
Output deviation voltage (Source output channel)	V,dev	Sout >=4.2V, Sout<=0.8V			20	mV	Note 4
		4.2V>Sout>0.8V			15	mV	
Output offset voltage	V_{OFSET}				35	mv	Note 6
Booster Operation							
Internal reference voltage	V_{REF}				1	%	Note 3
1st Booster (VDDx2) voltage	AVDD		4.75 *6)		5.5 *7)	V	Note 3
1st Booster (VDDx2) Drop voltage	VDDx2,drop	I_{AVDD} = 1.3mA (include Panel loading)			5%	%	Note 3
Linear range	V_{Linear}		0.2		AVDD-0.2	V	

Note 1: VDD1=1.6 to 3.6V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2, 3, 4: When the measurements are performed with LCD module, Measurement Points are like below.

Note 3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, PCLK, P/SX, VS, HS, DE, DIN, DOUT, SCL, GM1, GM0, LCM, RCM, P68, IM2, IM1, IM0, SRGB, SINV, SMX, SMY and Test pins

Note 5, Source channel loading= 15pF/channel, Gate channel loading= 50pF/channel.

Note 6, The Max. value is between with Note 4 measure point and Gamma setting value.

8.2. AC timing Characteristics

8.2.1. Parallel Interface Characteristics 18, 16 ,9 or 8-bits bus (8080-series MCU)

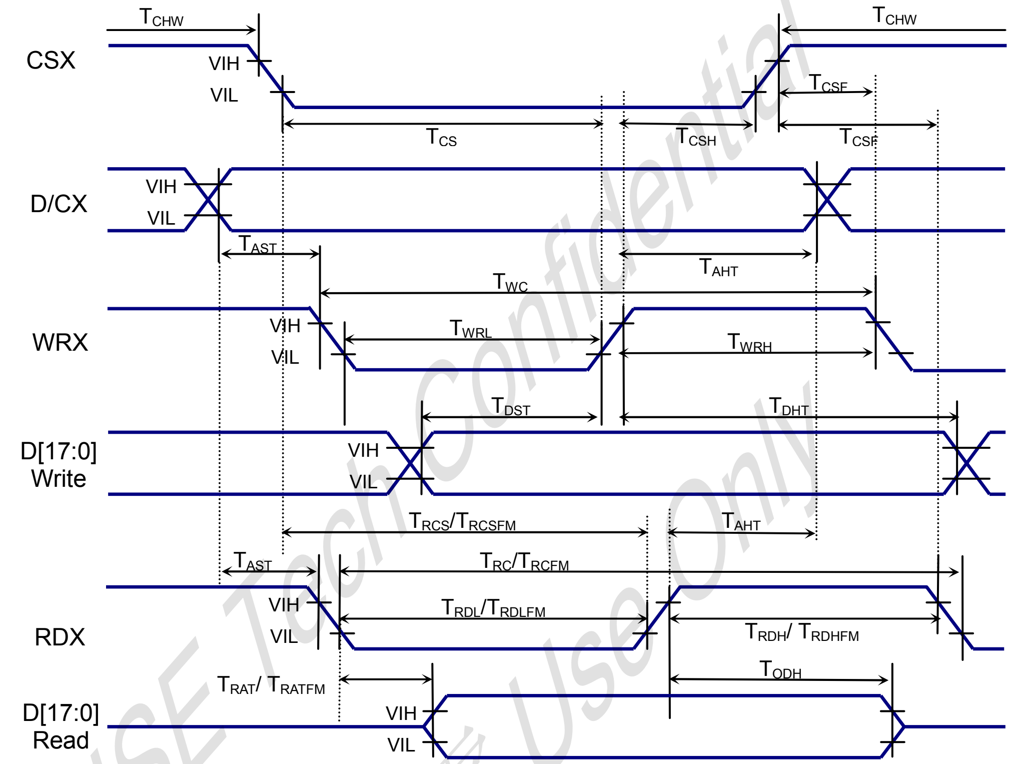


Fig. 8.2.1.1 Parallel Interface characteristics (8080-Series MCU)

Table 8.2.1.1: AC Characteristics for Parallel Interface18, 16, 9, 8-bits bus (8080-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-(3-transfer for one pixel)
	T_{CS}	Chip select setup time (Write)	35		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	100		ns	
	T_{WRH}	Control pulse "H" duration	35		ns	
	T_{WRL}	Control pulse "L" duration	35		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For maximum C_L=30pF For minimum C_L=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Note 1: VDD1=1.6 to 3.6V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

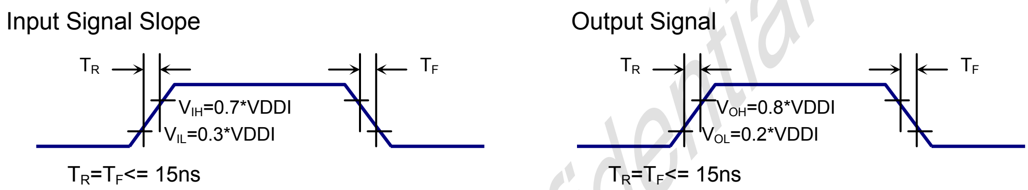


Fig. 8.2.1.2 Rising and Falling timing for Input and Output signal

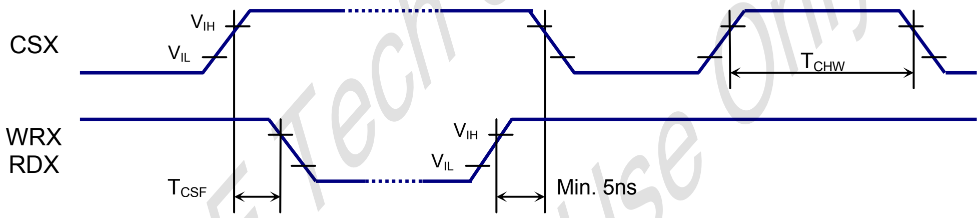


Fig.8.2.1.3 Chip selection (CSX) timing

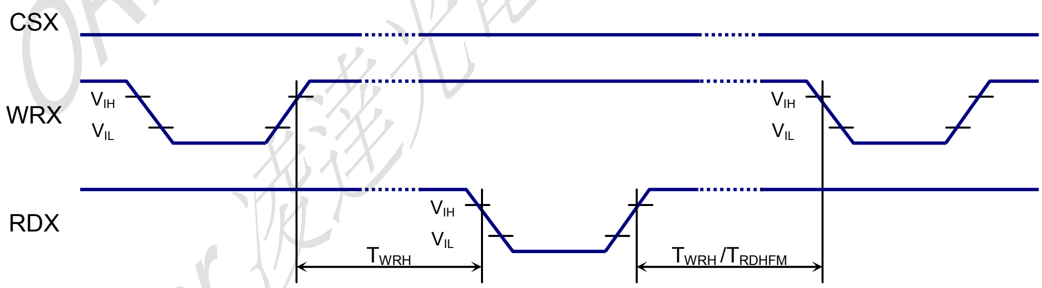


Fig. 8.2.1.4 Write to read and Read to write timing

NOTE: The input signal rise time and fall time (Tr, Tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.3. Parallel Interface Characteristics 18, 16 ,9 or 8-bits bus (6800-series MCU)

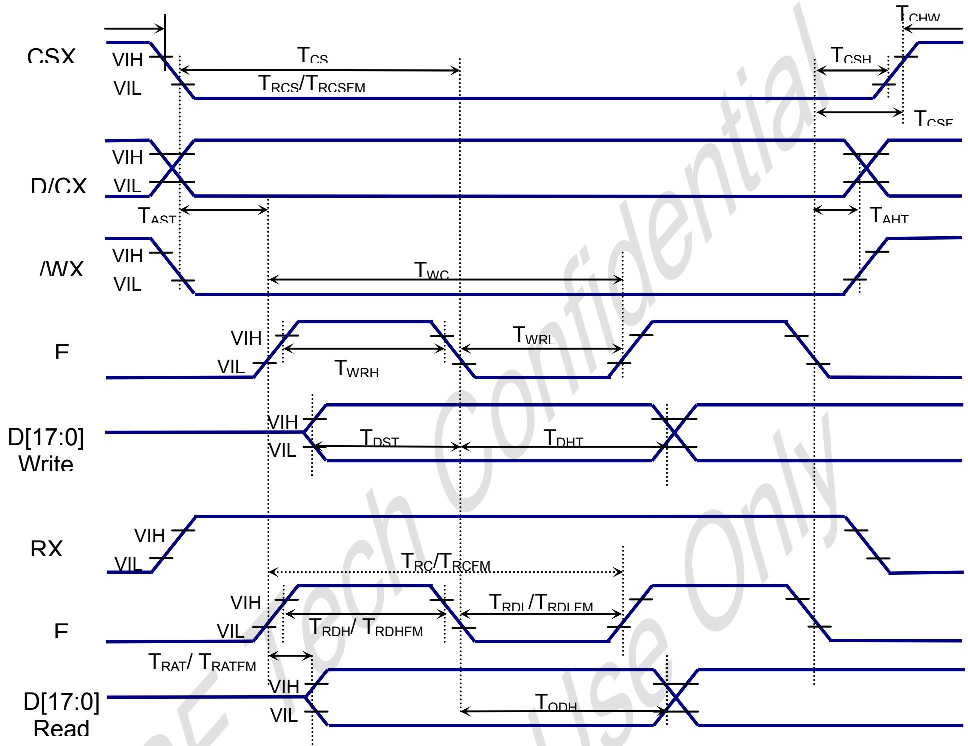


Fig. 8.3.1 Parallel Interface characteristics (6800-Series MCU)

Table 8.3.1: AC Characteristics for Parallel Interface 18, 16, 9, 8-bits bus (6800-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	35		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	100		ns	
	T_{WRH}	Control pulse "H" duration	35		ns	
	T_{WRL}	Control pulse "L" duration	35		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For maximum C_L=30pF For minimum C_L=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Note 1: VDD1=1.6 to 3.6V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.4. Serial Interface Characteristics (3-pin Serial)

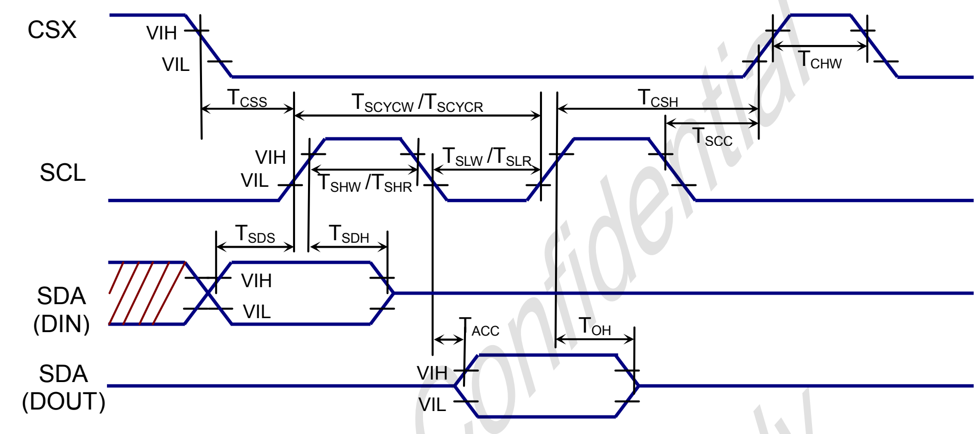


Fig. 8.4.1 3-pin Serial Interface Characteristics

Table 8.4.1: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	60		ns	
	T_{CSH}	Chip select hold time	65		ns	
	T_{SCC}	Chip select setup time	20		ns	
	T_{CHW}	Chip select setup time	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	100		ns	
	T_{SHW}	SCL "H" pulse width (Write)	35		ns	-
	T_{SLW}	SCL "L" pulse width (Write)	35		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN) (DOUT)	T_{SDS}	Data setup time	30		ns	
	T_{SDH}	Data hold time	30		ns	
	T_{ACC}	Access time	10		ns	For maximum C_L=30pF
	T_{OH}	Output disable time	15		ns	For minimum C_L=8pF

Note 1: VDD1=1.6 to 3.6V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

9. PAD LOCATIONS

9.1. PAD Assignment

Chip Information:

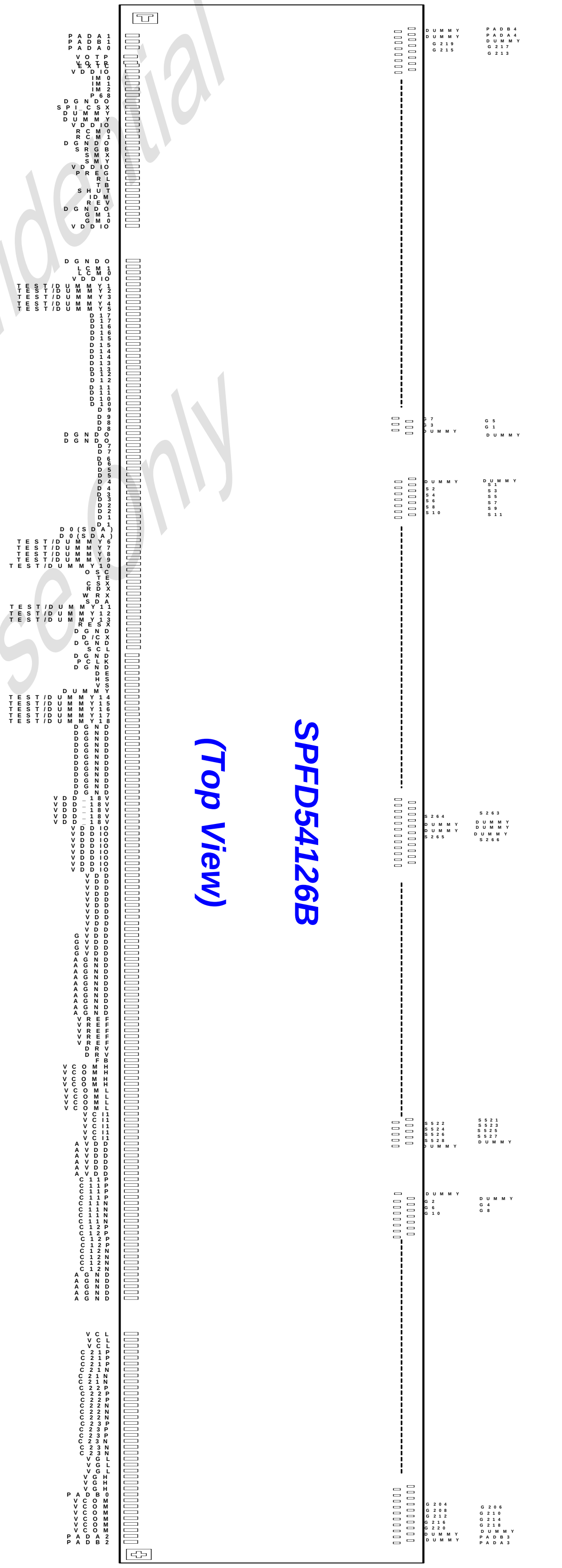
Basic Information:

Chip Size: 18650 um x 950 um

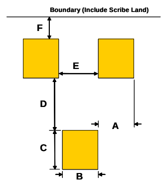
Chip thickness: 300um(Typ)

Coordinates origin: Pad Left-bottom side

Au Bump: Height = 15um (Typ)

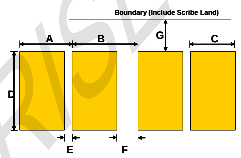


1. Output Pads



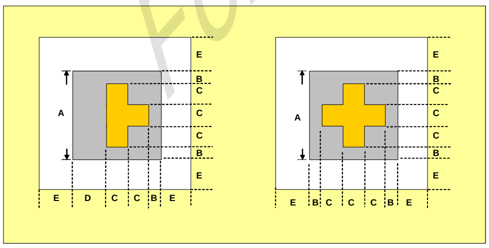
Item	Symbol	Size
Bump Pitch	A	23um
Bump Width	B	21um
Bump height	C	96um
Bump space 1	D	35um
Bump space 2	E	25um
Bump area	B x C	2016um^2
Chip boundary	F	45~70um

2. Input Pads



Item	Symbol	Size
Bump Pitch	A	64um
Bump Pitch1	B	80um
Bump Width	C	55um
Bump height	D	96um
Bump space 1	E	9um
Bump space 2	F	25um
Bump area	B x C	5280um^2
Chip boundary	G	45~70um

3. Alignment Marks



Al layer Clearance area Polyomide Gap

A	Symbol	Size
Alignment mark size	A	105um
Clearance gap1	B	15um
Clearance gap2	D	40um
Alignment mark width	C	25um
Alignment area	A x A	11025um^2
Gap width	E	40~48um

9.2. PAD Locations

	Name	X	Y
1	PADA1	125	93
2	PADB1	205	93
3	PADA0	285	93
4	VOTP	365	93
5	VOTP	445	93
6	EXTC	525	93
7	VDDIO	605	93
8	IM0	685	93
9	IM1	765	93
10	IM2	845	93
11	P68	925	93
12	DGNDO	1005	93
13	SPI_CSX	1085	93
14	Dummy	1165	93
15	Dummy	1245	93
16	VDDIO	1325	93
17	RCM0	1405	93
18	RCM1	1485	93
19	DGNDO	1565	93
20	SRGB	1645	93
21	SMX	1725	93
22	SMY	1805	93
23	VDDIO	1885	93
24	PREG	1965	93
25	RL	2045	93
26	TB	2125	93
27	SHUT	2205	93
28	IDM	2285	93
29	REV	2365	93
30	DGNDO	2445	93
31	GM1	2525	93
32	GM0	2605	93
33	VDDIO	2685	93
34	DGNDO	3165	93
35	LCM1	3245	93
36	LCM0	3325	93
37	VDDIO	3405	93
38	TEST/Dummy	3485	93
39	TEST/Dummy	3565	93
40	TEST/Dummy	3645	93
41	TEST/Dummy	3725	93
42	TEST/Dummy	3805	93
43	DB17	3885	93
44	DB17	3949	93
45	DB16	4029	93
46	DB16	4093	93
47	DB15	4173	93
48	DB15	4237	93
49	DB14	4317	93
50	DB14	4381	93
51	DB13	4461	93
52	DB13	4525	93
53	DB12	4605	93
54	DB12	4669	93
55	DB11	4749	93
56	DB11	4813	93
57	DB10	4893	93
58	DB10	4957	93
59	DB9	5037	93
60	DB9	5101	93
61	DB8	5181	93
62	DB8	5245	93
63	DGNDO	5325	93
64	DGNDO	5389	93
65	DB7	5469	93
66	DB7	5533	93
67	DB6	5613	93
68	DB6	5677	93
69	DB5	5757	93
70	DB5	5821	93
71	DB4	5901	93
72	DB4	5965	93
73	DB3	6045	93
74	DB3	6109	93
75	DB2	6189	93
76	DB2	6253	93
77	DB1	6333	93
78	DB1	6397	93
79	DB0	6477	93
80	DB0	6541	93
81	TEST/Dummy	6621	93
82	TEST/Dummy	6701	93
83	TEST/Dummy	6781	93
84	TEST/Dummy	6861	93
85	TEST/Dummy	6941	93
86	OSC	7021	93
87	TE	7101	93
88	CSX	7181	93
89	RDX	7261	93
90	WRX	7341	93
91	SDA	7421	93
92	TEST/Dummy	7501	93
93	TEST/Dummy	7581	93
94	TEST/Dummy	7661	93
95	RESX	7741	93
96	DGNDO	7821	93
97	DCX	7901	93
98	DGNDO	7981	93
99	SCL	8061	93
100	DGNDO	8141	93
101	PCLK	8221	93
102	DGNDO	8301	93
103	DE	8381	93
104	HS	8461	93
105	VS	8541	93
106	Dummy	8621	93
107	TEST/Dummy	8701	93
108	TEST/Dummy	8781	93
109	TEST/Dummy	8861	93
110	TEST/Dummy	8941	93
111	TEST/Dummy	9021	93
112	DGND	9101	93
113	DGND	9165	93
114	DGND	9229	93
115	DGND	9293	93
116	DGND	9357	93
117	DGND	9421	93
118	DGND	9485	93
119	DGND	9549	93
120	DGND	9613	93
121	DGND	9677	93
122	DGND	9741	93
123	DGND	9805	93
124	VCC	9885	93
125	VCC	9949	93
126	VCC	10013	93
127	VCC	10077	93
128	VCC	10141	93
129	VDDI	10221	93
130	VDDI	10285	93
131	VDDI	10349	93
132	VDDI	10413	93
133	VDDI	10477	93
134	VDDI	10541	93
135	VDDI	10605	93
136	VDDI	10669	93
137	VDD	10749	93
138	VDD	10813	93
139	VDD	10877	93
140	VDD	10941	93
141	VDD	11005	93
142	VDD	11069	93
143	VDD	11133	93
144	VDD	11197	93
145	VDD	11261	93
146	VDD	11325	93
147	GVDD	11405	93
148	GVDD	11469	93
149	GVDD	11533	93
150	GVDD	11597	93
151	AGND	11677	93
152	AGND	11741	93
153	AGND	11805	93
154	AGND	11869	93
155	AGND	11933	93
156	AGND	11997	93
157	AGND	12061	93
158	AGND	12125	93
159	AGND	12189	93
160	AGND	12253	93
161	VREF	12333	93
162	VREF	12397	93

	Name	X	Y
163	VREF	12461	93
164	VREF	12525	93
165	VREF	12589	93
166	DRV	12669	93
167	DRV	12749	93
168	FB	12829	93
169	VCOMH	12909	93
170	VCOMH	12973	93
171	VCOMH	13037	93
172	VCOMH	13101	93
173	VCOML	13181	93
174	VCOML	13245	93
175	VCOML	13309	93
176	VCOML	13373	93
177	VCI1	13453	93
178	VCI1	13517	93
179	VCI1	13581	93
180	VCI1	13645	93
181	VCI1	13709	93
182	AVDD	13789	93
183	AVDD	13853	93
184	AVDD	13917	93
185	AVDD	13981	93
186	AVDD	14045	93
187	AVDD	14109	93
188	C11P	14189	93
189	C11P	14253	93
190	C11P	14317	93
191	C11P	14381	93
192	C11N	14461	93
193	C11N	14525	93
194	C11N	14589	93
195	C11N	14653	93
196	C12P	14733	93
197	C12P	14797	93
198	C12P	14861	93
199	C12P	14925	93
200	C12N	15005	93
201	C12N	15069	93
202	C12N	15133	93
203	C12N	15197	93
204	AGND	15277	93
205	AGND	15341	93
206	AGND	15405	93
207	AGND	15469	93
208	AGND	15533	93
209	VCL	16013	93
210	VCL	16077	93
211	VCL	16141	93
212	C21P	16221	93
213	C21P	16285	93
214	C21P	16349	93
215	C21N	16429	93
216	C21N	16493	93
217	C21N	16557	93

	Name	X	Y
218	C22P	16637	93
219	C22P	16701	93
220	C22P	16765	93
221	C22N	16845	93
222	C22N	16909	93
223	C22N	16973	93
224	C23P	17053	93
225	C23P	17117	93
226	C23P	17181	93
227	C23N	17261	93
228	C23N	17325	93
229	C23N	17389	93
230	VGL	17469	93
231	VGL	17533	93
232	VGL	17597	93
233	VGH	17677	93
234	VGH	17741	93
235	VGH	17805	93
236	PADB0	17885	93
237	VCOM	17965	93
238	VCOM	18029	93
239	VCOM	18093	93
240	VCOM	18157	93
241	VCOM	18221	93
242	VCOM	18285	93
243	PADA2	18365	93
244	PADB2	18445	93
245	PADA3	18485	777
246	Dummy7	18462	646
247	PADB3	18439	777
248	Dummy8	18416	646
249	Dummy9	18393	777
250	G220	18370	646
251	G218	18347	777
252	G216	18324	646
253	G214	18301	777
254	G212	18278	646
255	G210	18255	777
256	G208	18232	646
257	G206	18209	777
258	G204	18186	646
259	G202	18163	777
260	G200	18140	646
261	G198	18117	777
262	G196	18094	646
263	G194	18071	777
264	G192	18048	646
265	G190	18025	777
266	G188	18002	646
267	G186	17979	777
268	G184	17956	646
269	G182	17933	777
270	G180	17910	646
271	G178	17887	777
272	G176	17864	646

	Name	X	Y
273	G174	17841	777
274	G172	17818	646
275	G170	17795	777
276	G168	17772	646
277	G166	17749	777
278	G164	17726	646
279	G162	17703	777
280	G160	17680	646
281	G158	17657	777
282	G156	17634	646
283	G154	17611	777
284	G152	17588	646
285	G150	17565	777
286	G148	17542	646
287	G146	17519	777
288	G144	17496	646
289	G142	17473	777
290	G140	17450	646
291	G138	17427	777
292	G136	17404	646
293	G134	17381	777
294	G132	17358	646
295	G130	17335	777
296	G128	17312	646
297	G126	17289	777
298	G124	17266	646
299	G122	17243	777
300	G120	17220	646
301	G118	17197	777
302	G116	17174	646
303	G114	17151	777
304	G112	17128	646
305	G110	17105	777
306	G108	17082	646
307	G106	17059	777
308	G104	17036	646
309	G102	17013	777
310	G100	16990	646
311	G98	16967	777
312	G96	16944	646
313	G94	16921	777
314	G92	16898	646
315	G90	16875	777
316	G88	16852	646
317	G86	16829	777
318	G84	16806	646
319	G82	16783	777
320	G80	16760	646
321	G78	16737	777
322	G76	16714	646
323	G74	16691	777
324	G72	16668	646
325	G70	16645	777
326	G68	16622	646
327	G66	16599	777

	Name	X	Y
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329	G62	16553	777
330	G60	16530	646
331	G58	16507	777
332	G56	16484	646
333	G54	16461	777
334	G52	16438	646
335	G50	16415	777
336	G48	16392	646
337	G46	16369	777
338	G44	16346	646
339	G42	16323	777
340	G40	16300	646
341	G38	16277	777
342	G36	16254	646
343	G34	16231	777
344	G32	16208	646
345	G30	16185	777
346	G28	16162	646
347	G26	16139	777
348	G24	16116	646
349	G22	16093	777
350	G20	16070	646
351	G18	16047	777
352	G16	16024	646
353	G14	16001	777
354	G12	15978	646
355	G10	15955	777
356	G8	15932	646
357	G6	15909	777
358	G4	15886	646
359	G2	15863	777
360	Dummy	15840	646
361	Dummy	15817	777
362	Dummy	15449	777
363	Dummy	15426	646
364	S528	15403	777
365	S527	15380	646
366	S526	15357	777
367	S525	15334	646
368	S524	15311	777
369	S523	15288	646
370	S522	15265	777
371	S521	15242	646
372	S520	15219	777
373	S519	15196	646
374	S518	15173	777
375	S517	15150	646
376	S516	15127	777
377	S515	15104	646
378	S514	15081	777
379	S513	15058	646
380	S512	15035	777
381	S511	15012	646
382	S510	14989	777

	Name	X	Y
383	S509	14966	646
384	S508	14943	777
385	S507	14920	646
386	S506	14897	777
387	S505	14874	646
388	S504	14851	777
389	S503	14828	646
390	S502	14805	777
391	S501	14782	646
392	S500	14759	777
393	S499	14736	646
394	S498	14713	777
395	S497	14690	646
396	S496	14667	777
397	S495	14644	646
398	S494	14621	777
399	S493	14598	646
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401	S491	14552	646
402	S490	14529	777
403	S489	14506	646
404	S488	14483	777
405	S487	14460	646
406	S486	14437	777
407	S485	14414	646
408	S484	14391	777
409	S483	14368	646
410	S482	14345	777
411	S481	14322	646
412	S480	14299	777
413	S479	14276	646
414	S478	14253	777
415	S477	14230	646
416	S476	14207	777
417	S475	14184	646
418	S474	14161	777
419	S473	14138	646
420	S472	14115	777
421	S471	14092	646
422	S470	14069	777
423	S469	14046	646
424	S468	14023	777
425	S467	14000	646
426	S466	13977	777
427	S465	13954	646
428	S464	13931	777
429	S463	13908	646
430	S462	13885	777
431	S461	13862	646
432	S460	13839	777
433	S459	13816	646
434	S458	13793	777
435	S457	13770	646
436	S456	13747	777
437	S455	13724	646

	Name	X	Y
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439	S453	13678	646
440	S452	13655	777
441	S451	13632	646
442	S450	13609	777
443	S449	13586	646
444	S448	13563	777
445	S447	13540	646
446	S446	13517	777
447	S445	13494	646
448	S444	13471	777
449	S443	13448	646
450	S442	13425	777
451	S441	13402	646
452	S440	13379	777
453	S439	13356	646
454	S438	13333	777
455	S437	13310	646
456	S436	13287	777
457	S435	13264	646
458	S434	13241	777
459	S433	13218	646
460	S432	13195	777
461	S431	13172	646
462	S430	13149	777
463	S429	13126	646
464	S428	13103	777
465	S427	13080	646
466	S426	13057	777
467	S425	13034	646
468	S424	13011	777
469	S423	12988	646
470	S422	12965	777
471	S421	12942	646
472	S420	12919	777
473	S419	12896	646
474	S418	12873	777
475	S417	12850	646
476	S416	12827	777
477	S415	12804	646
478	S414	12781	777
479	S413	12758	646
480	S412	12735	777
481	S411	12712	646
482	S410	12689	777
483	S409	12666	646
484	S408	12643	777
485	S407	12620	646
486	S406	12597	777
487	S405	12574	646
488	S404	12551	777
489	S403	12528	646
490	S402	12505	777
491	S401	12482	646
492	S400	12459	777

	Name	X	Y
493	S399	12436	646
494	S398	12413	777
495	S397	12390	646
496	S396	12367	777
497	S395	12344	646
498	S394	12321	777
499	S393	12298	646
500	S392	12275	777
501	S391	12252	646
502	S390	12229	777
503	S389	12206	646
504	S388	12183	777
505	S387	12160	646
506	S386	12137	777
507	S385	12114	646
508	S384	12091	777
509	S383	12068	646
510	S382	12045	777
511	S381	12022	646
512	S380	11999	777
513	S379	11976	646
514	S378	11953	777
515	S377	11930	646
516	S376	11907	777
517	S375	11884	646
518	S374	11861	777
519	S373	11838	646
520	S372	11815	777
521	S371	11792	646
522	S370	11769	777
523	S369	11746	646
524	S368	11723	777
525	S367	11700	646
526	S366	11677	777
527	S365	11654	646
528	S364	11631	777
529	S363	11608	646
530	S362	11585	777
531	S361	11562	646
532	S360	11539	777
533	S359	11516	646
534	S358	11493	777
535	S357	11470	646
536	S356	11447	777
537	S355	11424	646
538	S354	11401	777
539	S353	11378	646
540	S352	11355	777
541	S351	11332	646
542	S350	11309	777
543	S349	11286	646
544	S348	11263	777
545	S347	11240	646
546	S346	11217	777
547	S345	11194	646
548	S344	11171	777
549	S343	11148	646
550	S342	11125	777
551	S341	11102	646
552	S340	11079	777
553	S339	11056	646
554	S338	11033	777
555	S337	11010	646
556	S336	10987	777
557	S335	10964	646
558	S334	10941	777
559	S333	10918	646
560	S332	10895	777
561	S331	10872	646
562	S330	10849	777
563	S329	10826	646
564	S328	10803	777
565	S327	10780	646
566	S326	10757	777
567	S325	10734	646
568	S324	10711	777
569	S323	10688	646
570	S322	10665	777
571	S321	10642	646
572	S320	10619	777
573	S319	10596	646
574	S318	10573	777
575	S317	10550	646
576	S316	10527	777
577	S315	10504	646
578	S314	10481	777
579	S313	10458	646
580	S312	10435	777
581	S311	10412	646
582	S310	10389	777
583	S309	10366	646
584	S308	10343	777
585	S307	10320	646
586	S306	10297	777
587	S305	10274	646
588	S304	10251	777
589	S303	10228	646
590	S302	10205	777
591	S301	10182	646
592	S300	10159	777
593	S299	10136	646
594	S298	10113	777
595	S297	10090	646
596	S296	10067	777
597	S295	10044	646
598	S294	10021	777
599	S293	9998	646
600	S292	9975	777
601	S291	9952	646
602	S290	9929	777
603	S289	9906	646
604	S288	9883	777
605	S287	9860	646
606	S286	9837	777
607	S285	9814	646
608	S284	9791	777
609	S283	9768	646
610	S282	9745	777
611	S281	9722	646
612	S280	9699	777
613	S279	9676	646
614	S278	9653	777
615	S277	9630	646
616	S276	9607	777
617	S275	9584	646
618	S274	9561	777
619	S273	9538	646
620	S272	9515	777
621	S271	9492	646
622	S270	9469	777
623	S269	9446	646
624	S268	9423	777
625	S267	9400	646
626	S266	9377	777
627	S265	9354	646
628	Dummy	9331	777
629	Dummy	9308	646
630	Dummy	9285	777
631	Dummy	9262	646
632	Dummy	9239	777
633	S264	9216	646
634	S263	9193	777
635	S262	9170	646
636	S261	9147	777
637	S260	9124	646
638	S259	9101	777
639	S258	9078	646
640	S257	9055	777
641	S256	9032	646
642	S255	9009	777
643	S254	8986	646
644	S253	8963	777
645	S252	8940	646
646	S251	8917	777
647	S250	8894	646
648	S249	8871	777
649	S248	8848	646
650	S247	8825	777
651	S246	8802	646
652	S245	8779	777
653	S244	8756	646
654	S243	8733	777
655	S242	8710	646
656	S241	8687	777
657	S240	8664	646

	Name	X	Y
658	S239	8641	777
659	S238	8618	646
660	S237	8595	777
661	S236	8572	646
662	S235	8549	777
663	S234	8526	646
664	S233	8503	777
665	S232	8480	646
666	S231	8457	777
667	S230	8434	646
668	S229	8411	777
669	S228	8388	646
670	S227	8365	777
671	S226	8342	646
672	S225	8319	777
673	S224	8296	646
674	S223	8273	777
675	S222	8250	646
676	S221	8227	777
677	S220	8204	646
678	S219	8181	777
679	S218	8158	646
680	S217	8135	777
681	S216	8112	646
682	S215	8089	777
683	S214	8066	646
684	S213	8043	777
685	S212	8020	646
686	S211	7997	777
687	S210	7974	646
688	S209	7951	777
689	S208	7928	646
690	S207	7905	777
691	S206	7882	646
692	S205	7859	777
693	S204	7836	646
694	S203	7813	777
695	S202	7790	646
696	S201	7767	777
697	S200	7744	646
698	S199	7721	777
699	S198	7698	646
700	S197	7675	777
701	S196	7652	646
702	S195	7629	777
703	S194	7606	646
704	S193	7583	777
705	S192	7560	646
706	S191	7537	777
707	S190	7514	646
708	S189	7491	777
709	S188	7468	646
710	S187	7445	777
711	S186	7422	646
712	S185	7399	777
713	S184	7376	646
714	S183	7353	777
715	S182	7330	646
716	S181	7307	777
717	S180	7284	646
718	S179	7261	777
719	S178	7238	646
720	S177	7215	777
721	S176	7192	646
722	S175	7169	777
723	S174	7146	646
724	S173	7123	777
725	S172	7100	646
726	S171	7077	777
727	S170	7054	646
728	S169	7031	777
729	S168	7008	646
730	S167	6985	777
731	S166	6962	646
732	S165	6939	777
733	S164	6916	646
734	S163	6893	777
735	S162	6870	646
736	S161	6847	777
737	S160	6824	646
738	S159	6801	777
739	S158	6778	646
740	S157	6755	777
741	S156	6732	646
742	S155	6709	777
743	S154	6686	646
744	S153	6663	777
745	S152	6640	646
746	S151	6617	777
747	S150	6594	646
748	S149	6571	777
749	S148	6548	646
750	S147	6525	777
751	S146	6502	646
752	S145	6479	777
753	S144	6456	646
754	S143	6433	777
755	S142	6410	646
756	S141	6387	777
757	S140	6364	646
758	S139	6341	777
759	S138	6318	646
760	S137	6295	777
761	S136	6272	646
762	S135	6249	777
763	S134	6226	646
764	S133	6203	777
765	S132	6180	646
766	S131	6157	777
767	S130	6134	646
768	S129	6111	777
769	S128	6088	646
770	S127	6065	777
771	S126	6042	646
772	S125	6019	777
773	S124	5996	646
774	S123	5973	777
775	S122	5950	646
776	S121	5927	777
777	S120	5904	646
778	S119	5881	777
779	S118	5858	646
780	S117	5835	777
781	S116	5812	646
782	S115	5789	777
783	S114	5766	646
784	S113	5743	777
785	S112	5720	646
786	S111	5697	777
787	S110	5674	646
788	S109	5651	777
789	S108	5628	646
790	S107	5605	777
791	S106	5582	646
792	S105	5559	777
793	S104	5536	646
794	S103	5513	777
795	S102	5490	646
796	S101	5467	777
797	S100	5444	646
798	S99	5421	777
799	S98	5398	646
800	S97	5375	777
801	S96	5352	646
802	S95	5329	777
803	S94	5306	646
804	S93	5283	777
805	S92	5260	646
806	S91	5237	777
807	S90	5214	646
808	S89	5191	777
809	S88	5168	646
810	S87	5145	777
811	S86	5122	646
812	S85	5099	777
813	S84	5076	646
814	S83	5053	777
815	S82	5030	646
816	S81	5007	777
817	S80	4984	646
818	S79	4961	777
819	S78	4938	646
820	S77	4915	777
821	S76	4892	646
822	S75	4869	777

	Name	X	Y
823	S74	4846	646
824	S73	4823	777
825	S72	4800	646
826	S71	4777	777
827	S70	4754	646
828	S69	4731	777
829	S68	4708	646
830	S67	4685	777
831	S66	4662	646
832	S65	4639	777
833	S64	4616	646
834	S63	4593	777
835	S62	4570	646
836	S61	4547	777
837	S60	4524	646
838	S59	4501	777
839	S58	4478	646
840	S57	4455	777
841	S56	4432	646
842	S55	4409	777
843	S54	4386	646
844	S53	4363	777
845	S52	4340	646
846	S51	4317	777
847	S50	4294	646
848	S49	4271	777
849	S48	4248	646
850	S47	4225	777
851	S46	4202	646
852	S45	4179	777
853	S44	4156	646
854	S43	4133	777
855	S42	4110	646
856	S41	4087	777
857	S40	4064	646
858	S39	4041	777
859	S38	4018	646
860	S37	3995	777
861	S36	3972	646
862	S35	3949	777
863	S34	3926	646
864	S33	3903	777
865	S32	3880	646
866	S31	3857	777
867	S30	3834	646
868	S29	3811	777
869	S28	3788	646
870	S27	3765	777
871	S26	3742	646
872	S25	3719	777
873	S24	3696	646
874	S23	3673	777
875	S22	3650	646
876	S21	3627	777
877	S20	3604	646
878	S19	3581	777
879	S18	3558	646
880	S17	3535	777
881	S16	3512	646
882	S15	3489	777
883	S14	3466	646
884	S13	3443	777
885	S12	3420	646
886	S11	3397	777
887	S10	3374	646
888	S9	3351	777
889	S8	3328	646
890	S7	3305	777
891	S6	3282	646
892	S5	3259	777
893	S4	3236	646
894	S3	3213	777
895	S2	3190	646
896	S1	3167	777
897	Dummy	3144	646
898	Dummy	3121	777
899	Dummy	2753	777
900	Dummy	2730	646
901	G1	2707	777
902	G3	2684	646
903	G5	2661	777
904	G7	2638	646
905	G9	2615	777
906	G11	2592	646
907	G13	2569	777
908	G15	2546	646
909	G17	2523	777
910	G19	2500	646
911	G21	2477	777
912	G23	2454	646
913	G25	2431	777
914	G27	2408	646
915	G29	2385	777
916	G31	2362	646
917	G33	2339	777
918	G35	2316	646
919	G37	2293	777
920	G39	2270	646
921	G41	2247	777
922	G43	2224	646
923	G45	2201	777
924	G47	2178	646
925	G49	2155	777
926	G51	2132	646
927	G53	2109	777
928	G55	2086	646
929	G57	2063	777
930	G59	2040	646
931	G61	2017	777
932	G63	1994	646
933	G65	1971	777
934	G67	1948	646
935	G69	1925	777
936	G71	1902	646
937	G73	1879	777
938	G75	1856	646
939	G77	1833	777
940	G79	1810	646
941	G81	1787	777
942	G83	1764	646
943	G85	1741	777
944	G87	1718	646
945	G89	1695	777
946	G91	1672	646
947	G93	1649	777
948	G95	1626	646
949	G97	1603	777
950	G99	1580	646
951	G101	1557	777
952	G103	1534	646
953	G105	1511	777
954	G107	1488	646
955	G109	1465	777
956	G111	1442	646
957	G113	1419	777
958	G115	1396	646
959	G117	1373	777
960	G119	1350	646
961	G121	1327	777
962	G123	1304	646
963	G125	1281	777
964	G127	1258	646
965	G129	1235	777
966	G131	1212	646
967	G133	1189	777
968	G135	1166	646
969	G137	1143	777
970	G139	1120	646
971	G141	1097	777
972	G143	1074	646
973	G145	1051	777
974	G147	1028	646
975	G149	1005	777
976	G151	982	646
977	G153	959	777
978	G155	936	646
979	G157	913	777
980	G159	890	646
981	G161	867	777
982	G163	844	646
983	G165	821	777
984	G167	798	646
985	G169	775	777
986	G171	752	646
987	G173	729	777

	Name	X	Y
988	G175	706	646
989	G177	683	777
990	G179	660	646
991	G181	637	777
992	G183	614	646
993	G185	591	777
994	G187	568	646
995	G189	545	777
996	G191	522	646
997	G193	499	777
998	G195	476	646

	Name	X	Y
999	G197	453	777
1000	G199	430	646
1001	G201	407	777
1002	G203	384	646
1003	G205	361	777
1004	G207	338	646
1005	G209	315	777
1006	G211	292	646
1007	G213	269	777
1008	G215	246	646
1009	G217	223	777

	Name	X	Y
1010	G219	200	646
1011	Dummy	177	777
1012	Dummy	154	646
1013	PADA4	131	777
1014	Dummy	108	646
1015	PADB4	85	777

9.3. Wiring Resistance

No.	Name	Resistance	Priority
1	PADA1	open	4
2	PADB1	open	4
3	PADA0	(200 ohm)	4
4	VOTP	10 ohm	3
5	VOTP		
6	EXTC	200 ohm	4
7	VDDIO	open	4
8	IM0	200 ohm	4
9	IM1	200 ohm	4
10	IM2	200 ohm	4
11	P68	200 ohm	4
12	DGNDO	open	4
13	SPI_CSX	100 ohm	4
14	Dummy	open	4
15	Dummy	open	4
16	VDDIO	open	4
17	RCM0	200 ohm	4
18	RCM1	200 ohm	4
19	DGNDO	open	4
20	SRGB	200 ohm	4
21	SMX	200 ohm	4
22	SMY	200 ohm	4
23	VDDIO	open	4
24	PREG	open	4
25	RL	200 ohm	4
26	TB	200 ohm	4
27	SHUT	200 ohm	4
28	IDM	200 ohm	4
29	REV	200 ohm	4
30	DGNDO	open	4
31	GM1	200 ohm	4
32	GM0	200 ohm	4
33	VDDIO	open	4
34	DGNDO	open	4
35	LCM1	200 ohm	4
36	LCM0	200 ohm	4
37	VDDIO	open	4
38	TEST/Dummy	open	4
39	TEST/Dummy	open	4
40	TEST/Dummy	open	4
41	TEST/Dummy	open	4
42	TEST/Dummy	open	4
43	DB17	100 ohm	4
44	DB17		
45	DB16	100 ohm	4
46	DB16		
47	DB15	100 ohm	4
48	DB15		
49	DB14	100 ohm	4
50	DB14		
51	DB13	100 ohm	4
52	DB13		
53	DB12	100 ohm	4
54	DB12		
55	DB11	100 ohm	4
56	DB11		
57	DB10	100 ohm	4
58	DB10		
59	DB9	100 ohm	4
60	DB9		
61	DB8	100 ohm	4
62	DB8		
63	DGNDO	open	4
64	DGNDO	open	4
65	DB7	100 ohm	4
66	DB7		
67	DB6	100 ohm	4
68	DB6		
69	DB5	100 ohm	4
70	DB5		
71	DB4	100 ohm	4
72	DB4		
73	DB3	100 ohm	4
74	DB3		
75	DB2	100 ohm	4
76	DB2		
77	DB1	100 ohm	4
78	DB1		
79	DB0	100 ohm	4
80	DB0		
81	TEST/Dummy	open	4
82	TEST/Dummy	open	4
83	TEST/Dummy	open	4
84	TEST/Dummy	open	4
85	TEST/Dummy	open	4
86	OSC	open	4
87	TE	100 ohm	4
88	CSX	100 ohm	4
89	RDX	100 ohm	4
90	WRX	100 ohm	4
91	SDA	100 ohm	4
92	TEST/Dummy	open	4
93	TEST/Dummy	open	4
94	TEST/Dummy	open	4
95	RESX	200 ohm	4
96	DGNDO	open	4
97	DCX	100 ohm	4
98	DGNDO	open	4
99	SCL	100 ohm	4
100	DGNDO	open	4
101	PCLK	100 ohm	4
102	DGNDO	open	4
103	DE	100 ohm	4
104	HS	100 ohm	4
105	VS	100 ohm	4
106	Dummy	open	4
107	TEST/Dummy	open	4
108	TEST/Dummy	open	4
109	TEST/Dummy	open	4
110	TEST/Dummy	open	4
111	TEST/Dummy	open	4
112	DGND	10 ohm	1
113	DGND		
114	DGND		
115	DGND		
116	DGND		
117	DGND		
118	DGND		
119	DGND		
120	DGND		
121	DGND		
122	DGND		
123	DGND		
124	VCC	10 ohm	2
125	VCC		
126	VCC		
127	VCC		
128	VCC		
129	VDDI	10 ohm	2
130	VDDI		
131	VDDI		
132	VDDI		
133	VDDI		
134	VDDI		
135	VDDI		
136	VDDI		
137	VDD	10 ohm	1
138	VDD		
139	VDD		
140	VDD		
141	VDD	10 ohm	1
142	VDD		
143	VDD		
144	VDD		
145	VDD		
146	VDD		
147	GVDD	20 ohm	3
148	GVDD		
149	GVDD		
150	GVDD		
151	AGND	10 ohm	1
152	AGND		
153	AGND		
154	AGND		
155	AGND		
156	AGND		
157	AGND		
158	AGND		
159	AGND		
160	AGND		
161	VREF	10 ohm	3
162	VREF		

	Name	Resistance	Priority
163	VREF		
164	VREF		
165	VREF		
166	DRV	(30 ohm)	3
167	DRV		
168	FB	(30 ohm)	4
169	VCOMH	30 ohm	2
170	VCOMH		
171	VCOMH		
172	VCOMH		
173	VCOML	30 ohm	2
174	VCOML		
175	VCOML		
176	VCOML		
177	VCI1	10 ohm	2
178	VCI1		
179	VCI1		
180	VCI1		
181	VCI1		
182	AVDD	20 ohm	1
183	AVDD		
184	AVDD		
185	AVDD		
186	AVDD		
187	AVDD		
188	C11P	10 ohm	2
189	C11P		
190	C11P		
191	C11P		
192	C11N	10 ohm	2
193	C11N		

	Name	Resistance	Priority
194	C11N		
195	C11N		
196	C12P	10 ohm	2
197	C12P		
198	C12P		
199	C12P		
200	C12N	10 ohm	2
201	C12N		
202	C12N		
203	C12N		
204	AGND	10 ohm	1
205	AGND		
206	AGND		
207	AGND		
208	AGND		
209	VCL	20 ohm	3
210	VCL		
211	VCL	20 ohm	3
212	C21P	30 ohm	3
213	C21P		
214	C21P		
215	C21N	30 ohm	3
216	C21N		
217	C21N		
218	C22P	30 ohm	3
219	C22P		
220	C22P		
221	C22N	30 ohm	3
222	C22N		
223	C22N		
224	C23P	30 ohm	3

	Name	Resistance	Priority
225	C23P		
226	C23P		
227	C23N	30 ohm	3
228	C23N		
229	C23N		
230	VGL	10 ohm	2
231	VGL	10 ohm	2
232	VGL		
233	VGH	10 ohm	2
234	VGH		
235	VGH		
236	PADB0	(200 ohm)	4
237	VCOM	10 ohm	1
238	VCOM		
239	VCOM		
240	VCOM		
241	VCOM		
242	VCOM		
243	PADA2	open	4
244	PADB2	open	4
245			
246			
247			
248			
249			
250			

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10. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 20, 2006	0.2	1. Change title: Package/PAD Locations to PAD Locations	220
		2. Modify 2. FEATURE	6
		3. Modify Table 6.1.2. (4) to (4) ~ (9)	20-22
		4. Modify Description of 6.3.19.	108
		5. Modify 6.3.22 Table	112.113
		6. Modify 6.3.23 Table	114.115
		7. Modify 6.3.23 Table	116.117
		8. Modify 6.3.23 Table	118.119
		9. Modify 6.3.23 Table	120.121
		10. Modify 6.3.23 Table	122.123
OCT. 26, 2006	0.1	Original	218