

# TC4431/TC4432

## **1.5A High-Speed 30V MOSFET Drivers**

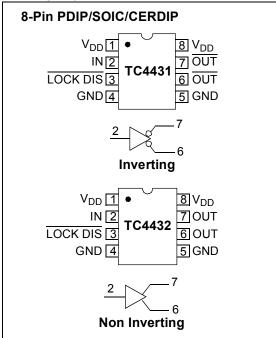
### Features

- High Peak Output Current 1.5A
- Wide Input Supply Voltage Operating Range:
  4.5V to 30V
- High Capacitive Load Drive Capability:
  - 1000 pF in 25 nsec
- Short Delay Times <78 nsec Typ.
- · Low Supply Current:
  - With Logic '1' Input 2.5 mA
  - With Logic '0' Input 300 µA
- Low Output Impedance  $7\Omega$
- Latch-Up Protected: Will Withstand >300 mA Reverse Current
- ESD Protected 4 kV

## Applications

- Small Motor Drive
- Power MOSFET Driver
- Driving Bipolar Transistors

### **Package Types**

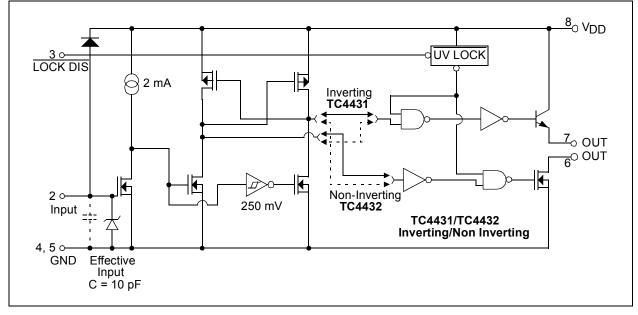


## **General Description**

The TC4431/TC4432 are 30V CMOS buffer/drivers suitable for use in high-side driver applications. They will not latch-up under any conditions within their power and voltage ratings. They can accept, without damage or logic upset, up to 300 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4 kV of electrostatic discharge.

Undervoltage lockout circuitry forces the output to a 'low' state when the input supply voltage drops below 7V. For operation at lower voltages, disable the lockout and start-up circuit by grounding pin 3 (LOCK DIS); for all other situations, pin 3 should be left floating. The under-voltage lockout and start-up circuit gives brownout protection when driving MOSFETS.

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

## **Absolute Maximum Ratings†**

Supply Voltage
Input Voltage (Note 1)V <sub>DD</sub> + 0.3V to GND
Package Power Dissipation ( $T_A \le 70^{\circ}C$ )
PDIP
CERDIP
SOIC470 mW
Maximum Junction Temperature, T <sub>J</sub> +150°C
Storage Temperature Range65°C to +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## **DC CHARACTERISTICS**

Electrical Specifications: Un	less other	wise noted, T <sub>A</sub>	, = +25°C wi	th 4.5V	$\leq V_{DD} \leq$	≤ 30V.
Parameters	Sym	Min	Тур	Мах	Units	Conditions
Input						
Logic '1', High Input Voltage	V <sub>IH</sub>	2.4	—		V	
Logic '0', Low Input Voltage	V <sub>IL</sub>	—	—	0.8	V	
Input Current (Note 1)	I <sub>IN</sub>	-1	—	1	μA	$0V \le V_{IN} \le 12V$
Output						
High Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> – 1.0	V <sub>DD</sub> – 0.8		V	I <sub>OUT</sub> = 100 mA
Low Output Voltage	V <sub>OL</sub>	_	_	0.025	V	
Output Resistance	R <sub>O</sub>	_	7	10	Ω	I <sub>OUT</sub> = 10 mA, V <sub>DD</sub> = 30V
Peak Output Current	I <sub>PK</sub>	_	3.0		Α	Source: V <sub>DD</sub> = 30V
			1.5			Sink: V <sub>DD</sub> = 30V
Latch-Up Protection	I <sub>REV</sub>	—	0.3	—	А	Duty cycle $\leq$ 2%, t $\leq$ 300 µsec
Withstand Reverse Current						
Switching Time (Note 2)						
Rise Time	t <sub>R</sub>	—	25	40	nsec	Figure 4-1
Fall Time	t <sub>F</sub>	—	33	50	nsec	Figure 4-1
Delay Time	t <sub>D1</sub>	_	62	80	nsec	Figure 4-1
Delay Time	t <sub>D2</sub>	_	78	90	nsec	Figure 4-1
Power Supply	•					
Power Supply Current	ا <sub>S</sub>	—	2.5	4	mA	V <sub>IN</sub> = 3V
	-		0.3	0.4		$V_{IN} = 0V$
Start-up Threshold	V <sub>S</sub>	_	8.4	10	V	
Drop-out Threshold	V <sub>DO</sub>	7	7.7		V	Note 3

**Note 1:** For inputs >12V, add a 1 k $\Omega$  resistor in series with the input. See "Typical Characteristics" graph for input current.

**2:** Switching times are ensured by design.

**3:** For operation below 7V, pin 3 (LOCK DIS) should be tied to ground to disable the lockout and start-up circuit, otherwise, pin 3 **must** be left floating.

## **DC CHARACTERISTICS (Continued)**

<b>Electrical Specifications:</b> Unless otherwise noted, Over operating temperature range with 4.5V $\leq$ V <sub>DD</sub> $\leq$ 30V.							
Parameters	Sym	Min	Тур	Max	Units	Conditions	
Input							
Logic '1', High Input Voltage	V <sub>IH</sub>	2.4	_	—	V		
Logic '0', Low Input Voltage	VIL	—	_	0.8	V		
Input Current (Note 1)	I <sub>IN</sub>	-10	_	10	μA	$0V \le V_{IN} \le 12V$	
Output							
High Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> – 1.2	_	_	V	I <sub>OUT</sub> = 100 mA	
Low Output Voltage	V <sub>OL</sub>	—	_	0.025	V		
Output Resistance	R <sub>O</sub>	—	_	12	Ω	I <sub>OUT</sub> = 10 mA, V <sub>DD</sub> = 30V	
Switching Time (Note 2)							
Rise Time	t <sub>R</sub>	—	_	60	nsec	Figure 4-1	
Fall Time	t <sub>F</sub>	—	_	70	nsec	Figure 4-1	
Delay Time	t <sub>D1</sub>	—	_	100	nsec	Figure 4-1	
Delay Time	t <sub>D2</sub>	—	_	110	nsec	Figure 4-1	
Power Supply	•			•		•	
Power Supply Current	ا <sub>S</sub>	—		6	mA	V <sub>IN</sub> = 3V	
		—		0.7		V <sub>IN</sub> = 0V	
Start-up Threshold	V <sub>S</sub>	—	8.4	10	V		
Drop-out Threshold	V <sub>DO</sub>	7	7.7	—	V	Note 3	

**Note 1:** For inputs >12V, add a 1 k $\Omega$  resistor in series with the input. See "Typical Characteristics" graph for input current.

2: Switching times are ensured by design.

**3:** For operation below 7V, pin 3 (LOCK DIS) should be tied to ground to disable the lockout and start-up circuit, otherwise, pin 3 **must** be left floating.

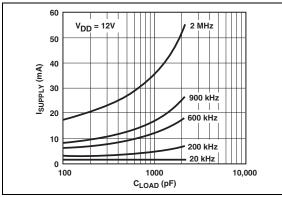
## **TEMPERATURE CHARACTERISTICS**

<b>Electrical Specifications:</b> Unless otherwise noted, all parameters apply with 4.5V $\leq$ V <sub>DD</sub> $\leq$ 30V.								
Parameters	Sym	Min	Тур	Мах	Units	Conditions		
Temperature Ranges								
Specified Temperature Range (C)	T <sub>A</sub>	0	—	+70	°C			
Specified Temperature Range (E)	T <sub>A</sub>	-40	—	+85	°C			
Maximum Junction Temperature	TJ	_	—	+150	°C			
Storage Temperature Range	T <sub>A</sub>	-65	—	+150	°C			
Package Thermal Resistances								
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	_	155	—	°C/W			
Thermal Resistance, 8L-PDIP	$\theta_{JA}$		125		°C/W			
Thermal Resistance, 8L-CERDIP	$\theta_{JA}$		150		°C/W			

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated,  $T_A = +25^{\circ}C$  with  $4.5V \le V_{DD} \le 30V$ .



*FIGURE 2-1:* Supply Current vs. Capacitive Load.

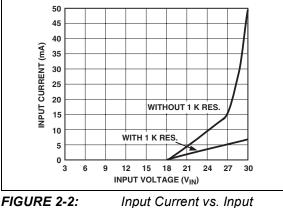
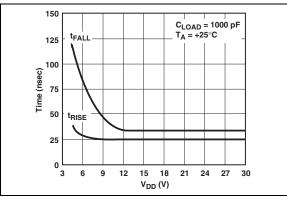
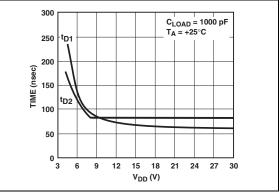


FIGURE 2-2: Inp Voltage.





Rise/Fall Time vs. V<sub>DD</sub>.



**FIGURE 2-4:**  $t_{D1}$  and  $t_{D2}$  Delay vs.  $V_{DD}$ .

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

Pin No.	Symbol	Description
1	V <sub>DD</sub>	Supply Input, 4.5V to 30V
2	IN	TTL/CMOS Compatible Input
3	LOCK DIS	Input Pin, Enable/Disable for UV Lockout
4	GND	Ground
5	GND	Ground
6	OUT	Drive Output, Pull Down
7	OUT	Drive Output, Pull Up
8	V <sub>DD</sub>	Supply Input, 4.5V to 30V

## TABLE 3-1: PIN FUNCTION TABLE

## 3.1 Supply Input (V<sub>DD</sub>)

The V<sub>DD</sub> input is the bias supply input for the MOSFET driver and is rated for 4.5V to 30V with respect to the ground pins. The V<sub>DD</sub> input should be bypassed to ground with a local ceramic capacitor. The value of this capacitor should be chosen based on the capacitive load that is being driven.

## 3.2 Control Input (IN)

The MOSFET driver input is a TTL/CMOS compatible input with 250 mV of hysteresis between the high and low threshold voltages. If an input signal level of greater than 12V is applied to the device, a series current limiting resistor is recommended.

## 3.3 Lockout Disable (LOCK DIS)

The lockout pin enables/disables the undervoltage lock-out feature of the device. If undervoltage lockout is desired (output is not enabled until the bias voltage reaches 8.4V (typical) on the rising edge and is disabled when the bias voltage reaches 7.7V (typical) on the falling edge), the lockout pin should be left floating. If operation below 7V is desired, the lockout pin should be tied to ground.

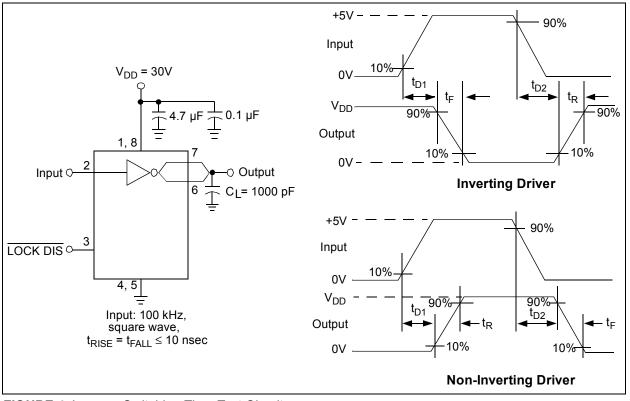
## 3.4 Ground (GND)

The ground pins are the return path for the bias current and for the high peak currents which discharge the load capacitor. Both ground pins should be used to ensure proper operation. The ground pins should be tied into a ground plane or have short traces to the bias supply source return.

## 3.5 Drive Output (OUT)

The TC4431/TC4432 devices have individual source and sink output pins. This feature can be used to adjust the rise and fall time independently by adding separate charge and discharge resistors external to the device. Pin 7 (source output) can source 3A peak currents into capacitive loads and pin 6 (sink output) can sink 1.5A peak currents from a capacitive load.

## 4.0 APPLICATIONS INFORMATION

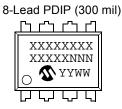




Switching Time Test Circuit.

## 5.0 PACKAGING INFORMATION

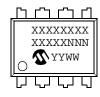
## 5.1 Package Marking Information

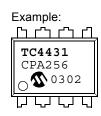


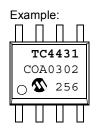
8-Lead SOIC (150 mil)



8-Lead CERDIP (300 mil)







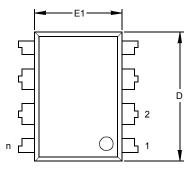
### Example:

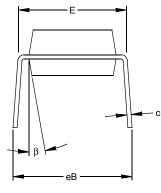


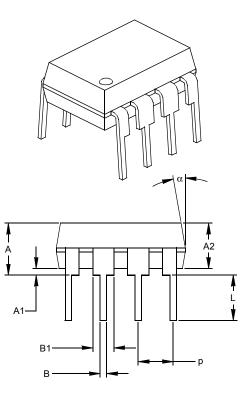
Legend	: XXX YY WW NNN	Customer specific information* Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code			
Note:	In the event the full Microchip part number cannot be marked on one line, it wi be carried over to the next line thus limiting the number of available characters for customer specific information.				

\* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)







	Units		INCHES*		Ν	<b>1ILLIMETERS</b>	3
Dimensio	n Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	Е	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

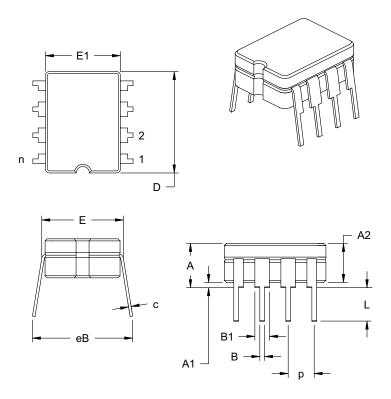
\* Controlling Parameter § Significant Characteristic

Notes: Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-001

Drawing No. C04-018

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## 8-Lead Ceramic Dual In-line (JA) – 300 mil (CERDIP)



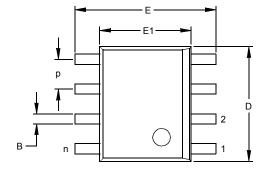
	Units		INCHES*		N	IILLIMETERS	
Dimensio	on Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	В	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

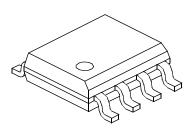
\*Controlling Parameter

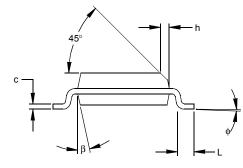
JEDEC Equivalent: MS-030

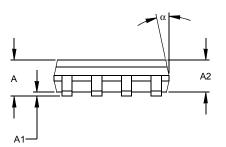
Drawing No. C04-010

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)









	Units		INCHES*		N	<b>1ILLIMETERS</b>	3
Dimensi	on Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.050			1.27	
Overall Height	Α	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	Е	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	¢	0	4	8	0	4	8
Lead Thickness	С	.008	.009	.010	0.20	0.23	0.25
Lead Width	В	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-012 Drawing No. C04-057

## TC4431/TC4432

NOTES:

## **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. Device	X /XX     Temperature Package Range	Exa a) b)	amples: TC4431COA: 1.5A MOSFET driver, SOIC package, 0°C to +70°C. TC4431EJA: 1.5A MOSFET driver, CEDD and Lances, 1000 to 10500
Device: Temperature Range:	TC4431: 1.5A High-Speed 30V MOSFET Driver, Inverting TC4432: 1.5A High-Speed 30V MOSFET Driver, Non Inverting $C = 0^{\circ}C \text{ to } +70^{\circ}C$ $E = -40^{\circ}C \text{ to } +85^{\circ}C$	a) b)	CERDIP package, -40°C to +85°C. TC4432CPA: 1.5A MOSFET driver, PDIP package, 0°C to +70°C. TC4432EPA: 1.5A MOSFET driver, PDIP package, -40°C to +85°C.
Package:	JA = Ceramic Dual In-line (300 mil Body), 8-lead * OA = Plastic SOIC, (150 mil Body), 8-lead OA713 = Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel) PA = Plastic DIP (300 mil Body), 8-lead * Offered in E-temp range only.		

### Sales and Support

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Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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## TC4431/TC4432

NOTES:

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### ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd Marketing Support Division Suite 22, 41 Rawson Street Epping 2121, NSW Australia Tel: 61-2-9868-6733 Fax: 61-2-9868-6755 China - Beijing Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office Unit 915 Bei Hai Wan Tai Bldg. No. 6 Chaoyangmen Beidajie Beijing, 100027, No. China Tel: 86-10-85282100 Fax: 86-10-85282104 China - Chengdu Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office Rm. 2401-2402, 24th Floor, Ming Xing Financial Tower No. 88 TIDU Street Chengdu 610016, China Tel: 86-28-86766200 Fax: 86-28-86766599

### China - Fuzhou

Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office Unit 28F, World Trade Plaza No. 71 Wusi Road Fuzhou 350001, China Tel: 86-591-7503506 Fax: 86-591-7503521

### China - Hong Kong SAR

Microchip Technology Hongkong Ltd. Unit 901-6, Tower 2, Metroplaza 223 Hing Fong Road Kwai Fong, N.T., Hong Kong Tel: 852-2401-1200 Fax: 852-2401-3431

China - Shanghai

Microchip Technology Consulting (Shanghai) Co., Ltd. Room 701, Bldg. B Far East International Plaza No. 317 Xian Xia Road Shanghai, 200051 Tel: 86-21-6275-5700 Fax: 86-21-6275-5060 **China - Shenzhen** 

Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office Rm. 1812, 18/F, Building A, United Plaza No. 5022 Binhe Road, Futian District Shenzhen 518033, China Tel: 86-755-82901380 Fax: 86-755-8295-1393

### China - Qingdao

Rm. B505A, Fullhope Plaza, No. 12 Hong Kong Central Rd. Qingdao 266071, China Tel: 86-532-5027355 Fax: 86-532-5027205 India Microchip Technology Inc. India Liaison Office Marketing Support Division Divyasree Chambers 1 Floor, Wing A (A3/A4) No. 11, O'Shaugnessey Road Bangalore, 560 025, India Tel: 91-80-2290061 Fax: 91-80-2290062

### Japan

Microchip Technology Japan K.K. Benex S-1 6F 3-18-20, Shinyokohama Kohoku-Ku, Yokohama-shi Kanagawa, 222-0033, Japan Tel: 81-45-471- 6166 Fax: 81-45-471-6122 Korea Microchip Technology Korea 168-1, Youngbo Bldg. 3 Floor Samsung-Dong, Kangnam-Ku Seoul, Korea 135-882 Tel: 82-2-554-7200 Fax: 82-2-558-5934 Singapore Microchip Technology Singapore Pte Ltd. 200 Middle Road #07-02 Prime Centre Singapore, 188980 Tel: 65-6334-8870 Fax: 65-6334-8850 Taiwan Microchip Technology (Barbados) Inc., Taiwan Branch 11F-3, No. 207 Tung Hua North Road Taipei, 105, Taiwan

Taipei, 105, Taiwan Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

## EUROPE

Austria Microchip Technology Austria GmbH Durisolstrasse 2 A-4600 Wels Austria Tel: 43-7242-2244-399 Fax: 43-7242-2244-393 Denmark Microchip Technology Nordic ApS Regus Business Centre

Lautrup hoj 1-3 Ballerup DK-2750 Denmark Tel: 45-4420-9895 Fax: 45-4420-9910

### France

Microchip Technology SARL Parc d'Activite du Moulin de Massy 43 Rue du Saule Trapu Batiment A - ler Etage 91300 Massy, France Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

### Germany

Microchip Technology GmbH Steinheilstrasse 10 D-85737 Ismaning, Germany Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 Italy

Microchip Technology SRL Via Quasimodo, 12 20025 Legnano (MI) Milan, Italy Tel: 39-0331-742611 Fax: 39-0331-466781 **United Kingdom** Microchip Ltd. 505 Eskdale Road Winnersh Triangle Wokingham Berkshire, England RG41 5TU Tel: 44-118-921-5869 Fax: 44-118-921-5820

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